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# Parametric System Model of a 112Gbps ADC-based SerDes for Architectural, Design & Validation Project Phases

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## Abstract

This paper presents a parametric ADC-based SerDes system modeling framework intended to support all project phases: from architectural definition, through analog and digital design, to validation.

Modeling techniques that enable a single model to support a wide range of system modeling activities are introduced. The parametrization of key design variables allows for the evaluation of architectural options to generate block level specifications. Object oriented modeling is used to decouple block interfaces from the evolving block implementation, thereby maintaining a simulation-ready top-level model. The block-level models support automated export to SystemVerlilog thereby facilitating mixed-signal design validation.

A correlation example is described to illustrate how the proposed modeling framework can be configured to reflect the IBIS-AMI model of a 112Gb/s ADC-based SerDes product.

In addition to being a valuable tool during SerDes development, these models can be delivered to system integrators enabling the incorporation of accurate models that capture the details of a real-life ADC-based SerDes right from the feasibility study phase. These models allow system integrators better observability and flexibility in performing end-to-end link analysis: including simulation of co-packaged and opto-electrical systems, and exploring interaction between SerDes and FEC. The underlying implementation can be obfuscated at different hierarchy levels for IP protection.

## Authors Biographies

**Aleksey Tyshchenko** is a co-founder of SeriaLink Systems – a consulting team focusing on system modeling of high-speed serial links, IBIS AMI modeling, model correlation and system validation. SeriaLink Systems is working on building a configurable modeling flow to support SerDes projects through their entire life cycles: from architecture definition, through analog and digital design, to design validation. He has been working on behavioral modeling of high-speed SerDes systems, architecture analysis, adaptation and signal integrity with multi-standards SerDes IP teams at V Semi and Intel. His Ph.D. research at the University of Toronto, Canada, focused on CDR systems for high-speed ADC-based receivers.

**David Halupka** is a co-founder of SeriaLink Systems. David has over 20 years of experience in hardware and embedded system design. He was with Kapik integration for 11 years, where he led Kapik's digital design team as Principal Engineer and Senior System-Architect. In 2018 David joined Intel's Mixed Signal-IP Group as Senior Systems Engineer, where he was involved in correlated modelling and adaptation algorithm

development for 56Gbps SerDes. Ph.D, M.A.Sc., and B.A.Sc. from the University of Toronto.

**Venu Balasubramonian** is responsible for Marvell's high speed PHY product line that encompasses Ethernet transceivers from 10G to 800G. Venu has 20+ years experience in the design, development and productization of high speed interconnect products and various other types of wireline and wireless modems. He has 20+ issued patents in the area of signal progressing architectures and adaptive signal processing algorithms. He is an active participant at IEEE 802.3 standards groups with multiple contributions to 10G, 25G and 100G Ethernet standards. Venu has an M.Tech in Electrical Engineering from Indian Institute of Technology, Kanpur.

**Lenin Patra** is a Marvell Fellow and CTO for the Networking PHY Business Unit – overseeing Base-T Copper PHY, High Speed SerDes PHY and Optical PHY product line. Lenin has more than 20 years of experience building the product architecture for Networking applications which encompasses High Speed SerDes products along with MACSec and PTP, Optical PHY products for intra datacenter applications, Base-T Copper PHY products for Enterprise applications. He has multiple patents in networking field.

# 1. Introduction

Throughout a SerDes IP development cycle, multiple SerDes system models at different levels of abstraction are required to guide development. First, a simplified system model is used for architectural exploration and to derive specifications for the main SerDes blocks. Then, a detailed system model is developed to capture main design aspects, and to evaluate design tradeoffs between blocks. This model is frequently populated with analog simulation data for correlation purposes, as analog design information becomes available. Finally, to support mixed-signal design validation, the behavior of analog blocks is captured in SystemVerilog models with circuit-representative interfaces. Very often, these three sets of SerDes models are developed by different parts of the development team, requiring some level of correlation, which, in turn, increases IP development overhead.

At the same time, two system modeling options are available to facilitate technical interaction between SerDes IP suppliers and system integrators. First, at the project onset, channel operating margin (COM) tool can be used to achieve high-level specification alignment. This alignment could be either within the context of communication standards, or outside standards for proprietary links. Communication standards, which use COM as a channel compliance tool, effectively define high-level SerDes performance guidelines in the form of a reference SerDes model and its parameters embedded in COM. Proprietary links can also leverage the COM reference SerDes to define performance targets. Then, as the SerDes IP development approaches completion, correlated IBIS-AMI models drive signal integrity (SI) simulations, which are typically performed by the system integrators – the IP consumers. IBIS-AMI models expose SerDes performance while obfuscating the implementation details within the IBIS standard constraints; hence, SerDes IP suppliers usually maintain IBIS-AMI development and correlation as stand-alone customer-facing efforts.

Between the COM-driven specification alignment and the IBIS-AMI-driven SI sign-off, however, simulation-based technical interaction between the SerDes IP providers and the system integrators is challenging due to the lack of adequate SerDes system models. The COM reference SerDes model lacks implementation-specific details and time-domain analysis capabilities; while the IBIS-AMI models limit system observability and require substantial update efforts. Hence, neither COM nor IBIS-AMI modeling options are sufficient to fully support SerDes providers and system integrators during their respective circuit and channel design phases.

In leading-edge high-speed serial link systems, the SerDes circuit development is frequently concurrent with the channel development, opening an opportunity to co-optimize the circuit and the channel designs for early standard-compliant systems, as well as for the proprietary links. At first glance, the detailed design-representative system model seems like a good candidate to facilitate this circuit–channel co-optimization. However, IP protection concerns along with model support logistic challenges typically prevent IP suppliers from sharing their internal system models with system integrators.

This paper presents a parametric ADC-based SerDes system modeling framework

intended to support all project phases: from architectural definition, through analog and digital design, to design validation. Furthermore, this modeling framework fills the gap between the generic COM and correlated IBIS-AMI models, enabling SerDes IP suppliers to provide high fidelity models to system integrators, earlier in the customer's system level design flow. This, in turn, enables simulation-based co-optimization between components of the serial link system.

We first introduce modeling techniques that enable a single model to support a wide range of system modeling activities. The parametrization of key design variables allows for the evaluation of a broad set of architectural solutions at the project onset, and to converge quickly on block-level specifications, facilitating the design phase. Decoupling relatively stable block interfaces from evolving block implementations enables a simulation-ready top-level system model at all times, while the underlying block-level implementations evolve to reflect the design's progress. We use object-oriented modeling to achieve this interface-implementation decoupling. The object-oriented approach also enables model obfuscation at the block level for IP protection when sharing the model with system integrators. The block-level models support automated export to C-code or stand-alone executables. This is accomplished via a minimal dependence on simulation environment solvers, facilitating mixed-signal design validation through auto-generated SystemVerilog behavioral models of analog blocks. Then, we describe a correlation example to illustrate how the proposed modeling framework can be configured to mimic a silicon correlated IBIS-AMI model for a 112 Gb/s ADC-based SerDes product.

The remainder of this paper is organized into six sections. Section 2 reviews typical system modeling activities through a SerDes IP development cycle, highlighting inefficiencies associated with maintaining multiple system models. Then, Section 3 outlines modeling techniques that enable a development of a unified SerDes modeling framework. Sections 4 and 5 present unified parametric transmitter and receiver models intended to support all internal SerDes development needs, and to augment customer-facing system modeling needs. Sections 6 describes a correlation example between the proposed SerDes model and an IBIS-AMI model of a 112 Gb/s ADC-based SerDes product, focusing on a customer-facing use case. Finally, Section 7 concludes this paper.

## 2. System Modeling through SerDes Development

The development of a multi-Gb/s SerDes, its integration into a high-speed communication product, and the successful deployment of this product is a multi-year endeavor that involves a multi-disciplinary engineering team across several participating companies. Through this time, engineers focus on their respective design areas using a wide range of tools and methodologies. Circuit designers, for instance, implement analog and digital SerDes blocks in a certain technology node using their corresponding CAD tools and circuit simulators. Meanwhile, board and package designers focus on the components of the communication channel heavily relying on electro-magnetic (EM) and signal integrity (SI) simulation tools. The multi-disciplinary nature of the engineering effort necessitates a careful coordination between design domains in order to deliver a successful high-speed communication project. As data rates reach 112 Gb/s and beyond –

thus making design targets more challenging – this coordination between engineering efforts across multiple disciplines and companies becomes ever more important.

SerDes system models facilitate such cross-disciplinary coordination in a quantitative and simulatable form at various stages of the project life cycle. System models enable interoperability simulations between individual components of the high-speed serial link system. Since system components are developed using different tools and workflows, these components need to be adequately abstracted into component models such that they can be co-simulated in a common environment.

In the example of SI simulations, the package and channel components are modeled as a set of S-parameters, which capture the frequency-dependent signal power propagation in these components, while abstracting away mechanical implementation details. The SerDes components are represented as IBIS-AMI models, which capture the SerDes equalization capabilities, while abstracting away the circuit implementation details. SI simulators serve as a common simulation environment, enabling co-simulation of the SerDes with different channels to verify if the SerDes equalization capabilities are sufficient to equalize the channel and achieve an adequate bit error rate (BER) in the system. In this particular example, the IBIS standard defines the interface between the SerDes models and the SI simulators. The IBIS standard also allows obfuscation of the SerDes implementation details for IP protection, which enables model exchange between different companies. This IP protection, however, comes at the cost of limited system observability in SI simulations.

Within the boundaries of a single company, where IP protection is not a concern, system-level simulations drive the verification of interaction between the analog and digital components of a SerDes, as well as the exploration of design trade-offs between various SerDes blocks. In this case, system models of the analog and digital blocks reflect the block functionality and structure in greater detail, using a high-level modeling environment, such as MATLAB or Simulink. The trend of using multiple SerDes system models to serve various purposes under different constraints is quite common. This practice, however, comes at the cost of maintaining multiple models of the same system at various levels of abstraction, and assuring that these models remain consistent with each other as the project evolves through its development cycle.

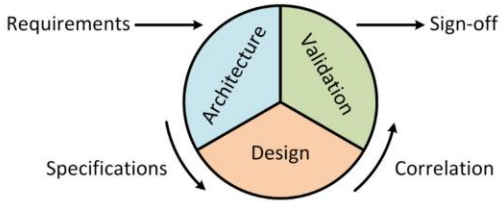


Figure 1. Three phases of SerDes development cycle

We can divide the SerDes development cycle into three major phases, as shown in Fig. 1, with different sets of system model supporting these three phases. First, the architectural exploration phase distills the project requirements into block-level specifications to

enable analog and digital design at block level. During this phase, system models at a high level of abstraction guide architectural choices, and the translation of project requirements into analog and digital specifications. The reference transmitter (TX) and receiver (RX) models in COM are examples of high-level models that are suitable for architectural exploration. Next, as block-level specifications are finalized, the analog and digital circuit design phase commences (Fig. 1). Meeting all block-level analog specifications is not always achievable in nano-scale technology nodes. At the same time, transistor-level simulations of the entire SerDes are prohibitively time consuming. Therefore, in this project phase, system models are essential to evaluate the design trade-offs and to refine block-level design targets. The system models intended to support the circuit design activities typically reflect the design details at a much finer level compared to the architectural models. Frequently, the circuit simulation data is fed into the system models to achieve a behavioral correlation between the system and the circuit models at the block level. Finally, as the design phase comes to an end, the mixed-signal validation phase starts. This project phase is intended to assure that the individual SerDes blocks – analog and digital – are interacting as expected, enabling project sign-off. Unlike system models used for architectural and design phases, the models used for the validation phase need to accurately reflect the interfaces at block boundaries, and they are typically implemented in SystemVerilog. Hence, multiple system models support the SerDes development activities within the SerDes supplier, before the SI simulations start on the system integrator's side. Maintaining multiple system models throughout the SerDes development life cycle comes at the cost of resource overhead and the need to assure that these models remain aligned with each other as the project evolves.

In the following section, we discuss modeling principles that enable the creation and maintenance of a single, unified system model capable of supporting all phases of the SerDes development cycle: from architectural exploration, through analog and digital design, to mixed-signal design validation. This model can also be used to drive early simulation-based technical engagement with the system integrators, providing the system observability that exceeds a typical IBIS-AMI simulation, thus enabling system integrators to explore serial link system aspects beyond a conventional SI analysis.

## 3. Unified System Modeling Framework

To enable a unified modeling approach, the SerDes system model needs to leverage commonalities between model use cases for the various project development phases. At the same time, the model needs to support an adjustable level of abstraction to allow both high-level modeling for architectural exploration, and low-level modeling for design trade-off evaluation. Furthermore, the model needs to be usable in multiple modeling environments to support the mixed-signal design validation phase. The visibility of implementation details also needs to be adjustable, for IP protection, to enable sharing of this model with system integrators.

We propose three modeling principles that jointly allow us to build unified SerDes models that satisfy the outlined requirements: object-oriented modeling, fixed-time-step modeling, and automated model export to low-level languages. These concepts are well-known and have been individually applied to programming and system modeling.

However, it is the combination of these principles in the context of SerDes modeling that enables us to build a unified modeling workflow. We will explore the impact of these principles on SerDes modeling in this section, and then exemplify the proposed modeling methodology through TX and RX models in the following sections.

Object-oriented modeling, at its essence, enables the decoupling of the model interface from its implementation. Throughout the SerDes development cycle, the data, clock, and control signal paths between primary components remain relatively constant. At the same time, the level of abstraction for every block – or its implementation – evolves. At the project onset, block-level models for architectural exploration typically start at a high level of abstraction, and they are populated with project specification data, or with expected and approximate performance data. As circuit design progresses, the level of abstraction for these blocks is refined, and models are populated with circuit simulation data to evaluate design trade-offs between blocks. Combining object-oriented modeling with adequate SerDes partitioning into primary blocks at a high level of the design hierarchy allows us to model these blocks as objects – or class instances – with constant and reusable interfaces, but with evolving underlying implementation details. Partitioning the system model into primary blocks, consistent to the circuit-level design partitioning, allows us to maintain stable interfaces between these blocks at a sufficiently high level of the design hierarchy without restricting the block's internal implementation. This enables maintaining a simple top-level model of the high-speed link throughout the entire development cycle. The primary benefit of this model is to explore the interaction between the system components, which is the common use case between architectural, design, and validation SerDes models. The progression from an abstract architectural to a detailed design-representative version of the model blocks is well-aligned with the object-oriented modeling approach, which allows modifications of the block implementation without disturbing its interface. The implementation details of individual blocks, or classes, can be obfuscated to ensure IP protection if the models are to be shared with system integrators. Hence, object-oriented modeling enables an adjustable level of abstraction and IP protection in the proposed unified SerDes modeling framework.

Fixed-time-step modeling is another key approach that allows using the proposed unified SerDes models in multiple simulations environments. Fixed-time-step modeling is a well-known technique that has been successfully used in the IBIS-AMI modeling environment. In this technique, continuous-time waveforms are represented as discrete-time samples with a constant sampling interval, which is sufficiently small to reflect the waveforms with adequate fidelity. Compared to variable-time-step modeling, where signals are updated at varying time intervals depending on the rate of change of these signals, the fixed-time-step modeling approach effectively shifts the role of the solver from the simulator to the model. In a sense, a simplified solver becomes embedded into the block-level model, reducing the role of the simulator from a differential solver to a fixed-interval scheduler, which triggers block updates. This allows the use of the proposed unified SerDes models and their individual blocks both in a high-level modeling environment, such as Simulink, and in event-driven simulation environment, such as Verilog, to drive mixed-signal validation. Moreover, the individual model blocks can be simulated using MATLAB test-benches (outside of Simulink) to leverage unit test

infrastructures and to enable continuous integration practices, which further simplify model maintenance and regression testing throughout the project lifecycle.

Even though fixed-time-step modeling is well-aligned with event-driven Verilog simulation concepts, it is insufficient by itself to enable the use the unified system models for mixed-signal validation since Verilog simulators do not directly support high-level modeling languages, such as MATLAB. To overcome this disconnect and to leverage the proposed models in the mixed-signal validation phase, we rely on automated export from a high-level modeling language (MATLAB) to a low-level language (C or C++), which can then be used in Verilog simulations using the direct programming interface (DPI). The resulting DPI models are directly compatible with mixed-signal validation workflows. Typically, a subset of features can be automatically converted from a high-level to a low-level language, and we limit ourselves only to this exportable subset as we build up the individual blocks of the unified SerDes model. The methodology described in [1] can be used to export all blocks in our proposed unified model to SystemVerilog.

In the following two sections, we leverage these presented modeling concepts to build parametric TX and RX for a 112 Gb/s ADC-based unified SerDes model suitable for all project development phases.

## 4. Parametric DAC-based TX Model

To build up the object-oriented TX for the unified SerDes model, we start by considering the parametrization of the reference TX in COM under IBIS-AMI modeling constraints, and then we present techniques to overcome these constraints, extending the model use cases well beyond typical SI simulations. Since COM is widely accepted in high-speed communication standards, such as Ethernet and OIF CEI, as the simulation tool to determine channel compliance with standard requirements, it makes sense to explore the level of parametrization in the COM reference TX model. After all, the process of defining the reference TX parameters can be seen as an architectural exploration of the practical channel and SerDes constraints to successfully converge to a communication standard. To enable such exploration, the reference TX parametrizes key design aspects that impact link performance. However, since representatives from all levels of the high-speed serial communication ecosystem participate in the standard development, the circuit implementation details remain abstracted away from the reference TX model in COM to prevent IP cross-contamination. COM absorbs the link performance penalties due to the SerDes circuit implementation in the form of an implementation margin, which is typically set to be 3 dB above the minimum SNR required for a target BER.

When it comes to SerDes circuit implementation, the architectural exploration phase typically initiates the project lifecycle. However, unlike the architectural exploration at the standard definition level, the goal of the architectural exploration for the circuit implementation is to map the standard-guided performance goals to block-level design specifications (see Fig. 1). In this context, COM parametrization of the reference TX is a good starting point to align with the standard definition, but it is insufficient to drive the block-level specifications since the circuit implementation details are abstracted away in COM. Furthermore, COM at its essence is a statistical simulation tool, which captures

linear time-invariant (LTI) link effects via the impulse response of the system, while non-linear and/or time-varying effects are accounted for through SNR penalties.

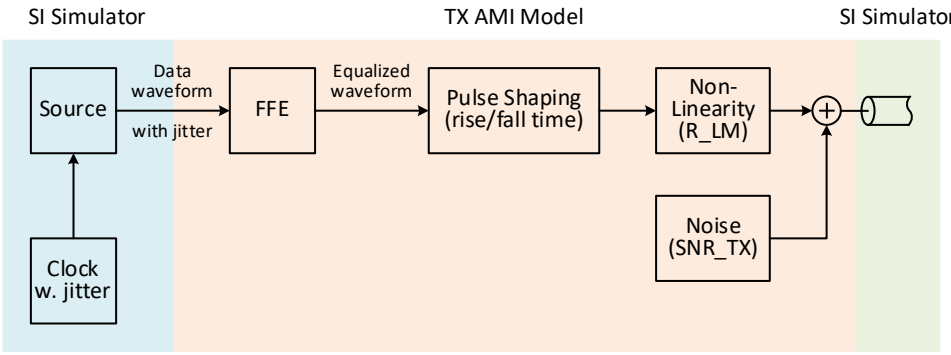


Figure 2. COM-parametric TX model in IBIS-AMI modeling workflow

To leverage COM reference TX parametrization, and to expand it beyond the standard definition into the circuit implementation domain, we start with the TX model within the constraints of the IBIS-AMI modeling framework, as shown in Fig. 2. In the SI simulator, clock triggers a data source to generate a data waveform with jitter for the TX model. The TX model then applies feed-forward equalization (FFE) to the incoming waveform to generate an equalized waveform. Next, a pulse-shaping filter limits the rise/fall time of the equalized waveform, and a non-linearity block adds the saturation effect to the waveform. Finally, noise is added to the TX waveform before it is fed into the channel. In this case, COM TX parametrization is shared between the SI simulator and the TX model. The SI simulator manages the clock jitter, the data sequence, and the modulation, while the TX model manages the equalization, rise/fall time, non-linearity and noise. This modeling approach adequately captures the COM level of TX parameterization, and it enables time-domain simulations to account for the non-linear and time-varying effects. However, this model is insufficient to drive block-level specifications since the TX implementation details are not reflected in this modeling approach.

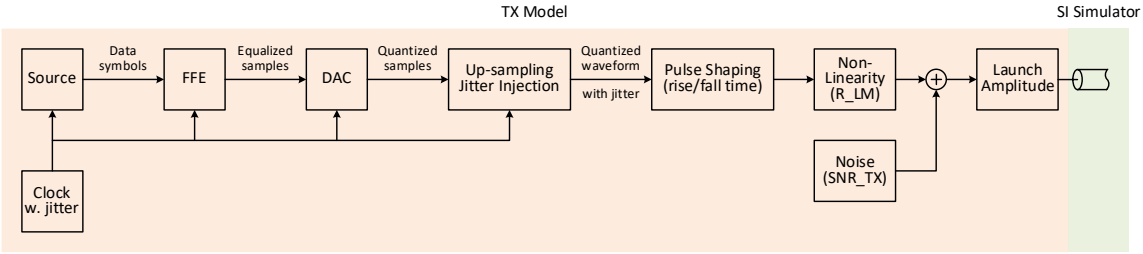


Figure 3. Proposed parametric DAC-based TX model

This brings us to the proposed parametric DAC-based TX model, presented in Fig. 3. In this model, instead of relying on the SI simulator, the TX model prepares the data stream and conditions it according to the TX implementation for link simulations. First, a clock with jitter triggers the data source. Since the model is not constrained by the IBIS-AMI framework, the model supports a wide range of jitter sources. To support jitter resolution, below the sampling interval in the fixed-time-step modeling approach, the clock needs to be continuous in amplitude (a sinusoid), which enables the use of interpolation to adjust

clock transitions to account for jitter. The data source then prepares data symbols for the simulations. The bit sequence is modulated into the symbol sequence, adding Gray coding, precoding, and reversing the bit order if necessary. The FFE, also triggered by the clock, converts data symbols into equalized samples. Access to the equalized samples, as opposed to the equalized waveform, enables the addition of a DAC, which quantizes the equalized samples in amplitude. Next, the TX model up-samples the equalized and quantized samples to form a continuous-time waveform. The TX model then adds the impact of rise/fall time, nonlinearity, and noise to the output waveform. Finally, the launch amplitude is adjusted using a broad-band gain without impacting the TX SNR.

In addition to reflecting the number of FFE taps and their ranges, the proposed TX model captures the effect of the DAC, which is a common architectural trend in recent high-speed SerDes [2–6]. Furthermore, since the TX model manages the source bit stream, it can now model FEC data encoding, including proprietary FEC algorithms.

Following the outlined methodology, we implemented the TX model in Simulink, as shown in Fig. 4. In this model, we use Simulink as a convenient high-level environment to integrate the individual blocks into the TX model, and to observe signals between the individual blocks. The blocks, however, are implemented as object-oriented MATLAB that is exportable to low-level languages (C or C++). These individual blocks are simulatable in their corresponding test-benches to support the continuous code integration and testing, and they are configured through scriptable workflows to enable regression simulations.

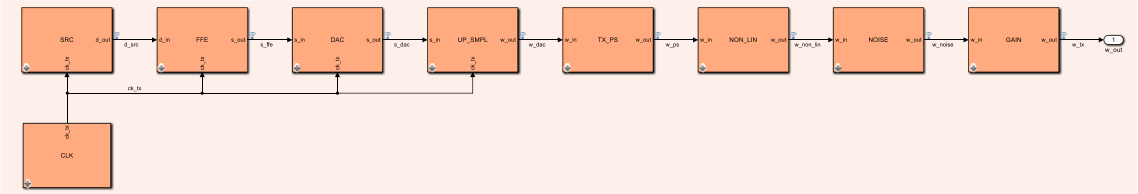


Figure 4. Proposed TX model in Simulink

The proposed TX model supports COM-like parametrization while enabling time-domain simulations that capture the circuit implementation details and non-idealities. As the project progresses, these non-idealities can be refined to reflect the circuit impact on system models and therefore explore design trade-offs. We now turn our attention to the RX model and follow the same modeling methodology.

## 5. Parametric ADC-based RX Model

To build a parametric RX for the unified SerDes modeling framework, we start with the parametrization of the reference RX in COM, and we partition the RX model into its primary blocks so that it is consistent with a typical circuit design. Fig. 5 illustrates an example of an ADC-based RX topology. First, a continuous time linear equalizer (CTLE) partially equalizes the received waveform, and a variable gain amplifier (VGA) adjusts the waveform's amplitude to match the dynamic range of the analog-to-digital converter (ADC). Then, a time-interleaved ADC, triggered by the recovered clock, samples the partially-equalized waveform at one sample per symbol, and quantizes these samples in

amplitude according to the ADC resolution. Next, the sequential ADC samples are demultiplexed into parallel frames of samples. The frame rate of these parallel samples matches the clock frequency of the subsequent digital signal processor (DSP) engine. In the DSP, which is typically implemented as a synthesized digital circuit, the feed-forward equalizer (FFE) and decision-feedback equalizer (DFE) further equalize the demultiplexed samples for data symbol recovery from the fully equalized samples. At the same time, the phase detector (PD) and loop filter (LF) recover the phase of the received signal to align the recovered clock with the symbol centers, thus closing the clock recovery loop. Finally, the adaptation engine monitors the residual inter-symbol interference (ISI) in the fully equalized samples and possibly other performance metrics, such as signal-to-noise ratio (SNR), to track the decision thresholds and to tune the equalization components in order to achieve a sufficiently low BER. The adaptation engine interacts with a microcontroller to manage link bring-up sequencing, link training, and possibly some of the RX adaptation algorithms in firmware.

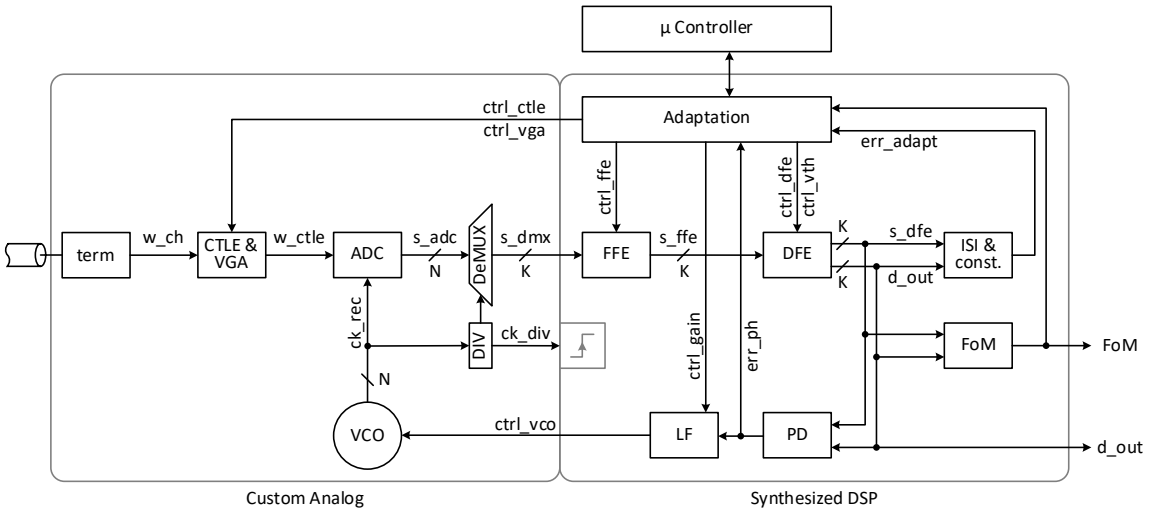


Figure 5. Block-diagram of an ADC-based RX

Since COM does not impose any implementation constraints, its reference RX is parametrized to reflect the RX equalization capabilities rather than the RX structure. We absorb the COM performance parametrization into the corresponding blocks of the proposed RX model. The CTLE frequency response and input-referred noise can be configured using COM CTLE parameters at the project onset. As the circuit design progresses, the same CTLE model can be refined with a design-representative noise and AC response. In a similar manner, the number of FFE and DFE taps, as well as their ranges, are parametrized consistently with COM.

In addition to COM-like performance parametrization, we built into the RX model a level of implementation-dependent parametrization that is beyond the scope of COM. The primary goal of this implementation-level parametrization is to enable the evaluation of essential design trade-offs in the architectural exploration phase early in the SerDes development. The depth of the ADC time interleaving and the size of the demultiplexed sample frames are examples of early architectural decisions that impact RX block-level

specifications. Increasing the time-interleaving depth, *N* in Fig. 5, relaxes the individual ADC requirements and reduces the recovered clock rate at the cost of increasing the number of recovered-clock phases, with stricter phase alignment and tighter matching requirements between the individual ADCs. Similarly, increasing the demultiplexed frame size, *K*, relaxes the DSP clock rate requirements at the cost of increasing the latency of the clock recovery loop, which, in turn, degrades loop stability. In the proposed RX model, we parametrized both these design variables, and the block interfaces that depend on these variables. As a result, the same RX model can first be used to evaluate trade-offs around these variables during architectural exploration, and then the model can be configured to reflect actual values during the circuit design phase. In addition to the time-interleaving depth, the ADC nominal and effective resolutions are also parametrized to explore the impact of the ADC resolution on the system performance, and to help converge on ADC specifications.

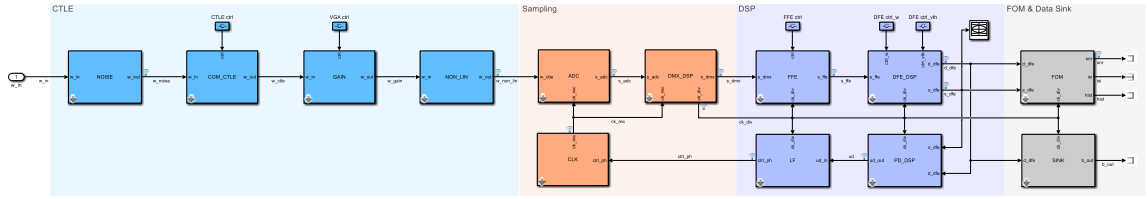


Figure 6. Proposed RX model in Simulink (adaptation blocks removed to simplify diagram)

To achieve a high level of performance and structural parametrization at block level, the individual blocks are modeled using the object-oriented MATLAB code. This code is then embedded into Simulink blocks that are connected to form the RX model, as shown in Fig. 6. By partitioning the model between Simulink and MATLAB, we leverage Simulink for the visual representation of the top-level connectivity and its signal observability, while taking the full advantage of MATLAB code flexibility to process parallel data sets with configurable set sizes.

In addition to supporting all phases of SerDes development, the proposed unified SerDes models can also facilitate simulation-based technical interaction between SerDes providers and system integrators. Nowadays, IBIS-AMI models serve as the de-facto means for providers to convey SerDes performance in a simulatable form to system integrators. ADC-based RX architectures, however, are challenging to model within the IBIS-AMI framework, which is intended for conventional analog-centric RX topologies, resulting in limited observability in SI simulations [7]. Moreover, it takes time to build, verify and correlate IBIS-AMI models based either on the internal SerDes models or lab measurements. Consequently, system integrators are gated by availability of the IBIS-AMI models from co-simulating their channel designs with the SerDes; thereby, increasing time to market. To alleviate this dependency, the proposed parametric SerDes models can be shared with system integrators to augment IBIS-AMI collaterals.

The modeling techniques at the core of the proposed parametric SerDes models make them a good option to enable early technical engagement between SerDes providers and system integrators. A combination of performance (COM-like) and implementation parameters allow for a quick configuration of the models in a high-level modeling

environment to reflect a particular SerDes design. SerDes suppliers typically share some architectural information and performance targets with system integrators as part of the technical SerDes evaluation. Our proposed modeling methodology leverages this information in the form of the model parameters to deliver simulation-ready SerDes models with minimal resource overhead. The resulting models can be delivered in a self-contained Simulink test-bench. Similar to the IBIS-AMI's IP protection capabilities, object-oriented modeling allows delivery of the block-level MATLAB models as obfuscated P-code. At the same time, the top-level RX model remains visible in Simulink, which assures system simulation observability well-beyond typical SI simulations with IBIS-AMI models. This extended system observability and the use of Simulink as the primary simulation environment enables the use of the proposed models for system-level analysis of SerDes with FEC, opto-electrical links, and co-packaged solutions – the types of system analysis that have traditionally been beyond the scope of IBIS-AMI models.

The following section presents an example configuration of the proposed parametric ADC-based model so that it correlates to the IBIS-AMI model for a 112 Gb/s SerDes product intended for LR applications.

## 6. Model Correlation

Correlation between the proposed parametric SerDes model and a 112 Gb/s ADC-based SerDes [6] is to demonstrate primarily that the proposed modeling framework can fill the void between COM and IBIS-AMI models for simulation-based technical interaction between SerDes providers and system integrators. For the external model use case, where IP protection is very important, we start with a set of generic, rather than design-specific, SerDes blocks. We then configure these blocks to reflect the SerDes IP design details and to achieve SNR and BER correlation across a test channel. In addition to highlighting the ease of model configuration, and correlation to performance result obtained from IBIS-AMI model, we illustrate the high level of the system behavior observability available to system integrators.

To configure the TX, we used a set of COM-like parameters, which were assigned values extracted from the SerDes design. These parameters also populate the IBIS-AMI model of the same SerDes at the end of the development cycle. Random and deterministic jitter (RJ and DJ) modulate the TX clock, which triggers the data source. The number and range of the FFE taps bounds the TX equalization within the SerDes capabilities. The rise/fall time (tr/tf) reflects the bandwidth limitations of the TX output stage. The level mismatch ratio (RLM) adds a saturating non-linearity effect to the output waveform, while the TX SNR determines the amount of additive noise present in the output waveform. A broad-band gain sets the TX launch amplitude without impacting the previously added non-idealities. On-die termination is absorbed into the channel response. Depending on the SerDes development progress, all of these parameters can either be locked inside the model or exposed, within reasonable bounds, to system integrators. This facilitates a thorough exploration of the SerDes performance in a real-life system environment. As an example, in addition to RJ and DJ, the TX model can be

configured to inject a wide range of other jitter sources, or to enable jitter tolerance simulations.

On the RX side, we configured the CTLE to reflect the circuit frequency response, and set a representative VGA gain range and granularity. The ADC effective resolution is set based on the design. The FFE and DFE are configured using COM-like parameters in terms of the number of taps and their ranges. When focusing on data path performance and SI simulations, a Mueller-Müller PD with a generic loop filter is sufficient, while the RX RJ and DJ approximate the jitter impact on the data path. As simulations advance towards jitter tolerance tests, the loop filter can be configured to adequately reflect clock recovery loop dynamics. Similar to the TX, the RX parameters can be either frozen inside the model or exposed to system integrators for exploratory purposes.

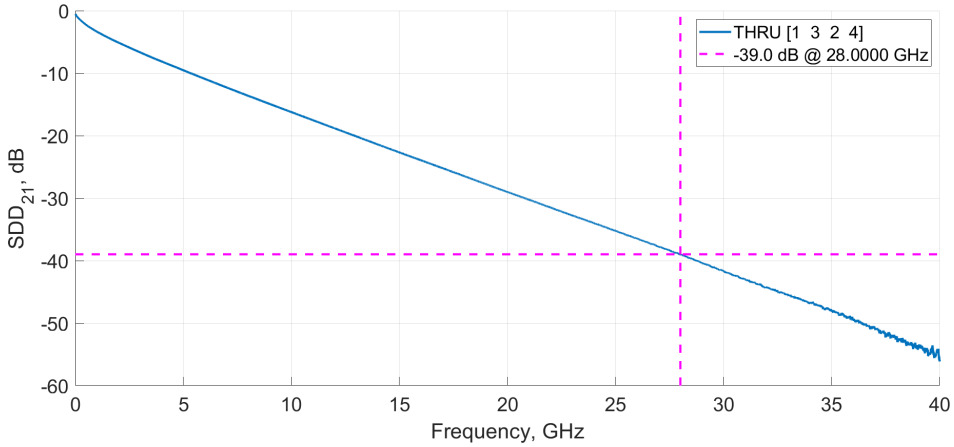


Figure 7. Channel response used for model correlation

After setting these TX and RX parameters to be consistent with the SerDes design and its correlated IBIS-AMI model, we ran simulations at 112 Gb/s across a 39 dB channel, shown in Fig. 7. The figure of merit (FoM) block in our model reports 21.5 dB SNR, which is consistent with the IBIS-AMI simulation result for the same channel, and correlates to the lab measured BER of $10^{-7}$.

In addition to the SNR, the FoM block tracks the residual ISI as the recovered clock phase converges, as illustrated in Fig. 8. This residual ISI provides additional insight into the performance limiting factors from a signal integrity point of view. Access to the distributions of the equalized samples – vertical histograms – allows us to evaluate the impact of non-linearities and the system sensitivity to amplitude compression as shown in Fig. 9, where the two histograms are plotted for two different non-linearity characteristics at the VGA output. In a similar way, all signals at the top level of the RX hierarchy can be easily observed since the model is assembled in the high-level Simulink environment, allowing for extensive monitoring capabilities. The model can be released in a self-contained package with a scriptable configuration flow to support regression simulations. As blocks are updated in pace with the SerDes design progress, or if additional blocks need to be shared with system integrators, the release and support overhead of the proposed modeling framework remains significantly lower than that of IBIS-AMI

models. This, in turn, allows for multiple model releases to system integrators throughout the design cycle, which tightens the technical interaction between the teams and enables co-optimization between SerDes and channel development.

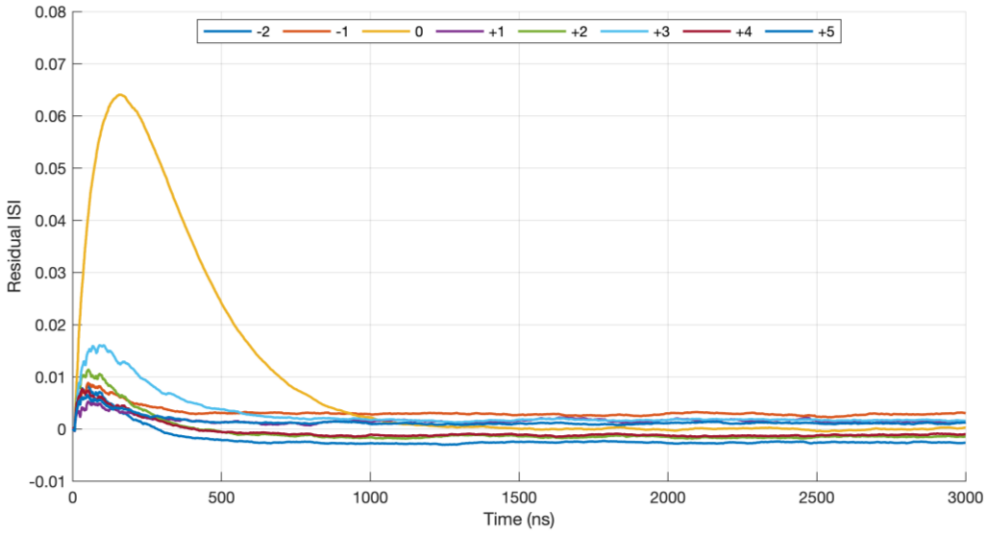


Figure 8. Residual ISI convergence, cursor (Tap 0) is plotted as deviation from target amplitude

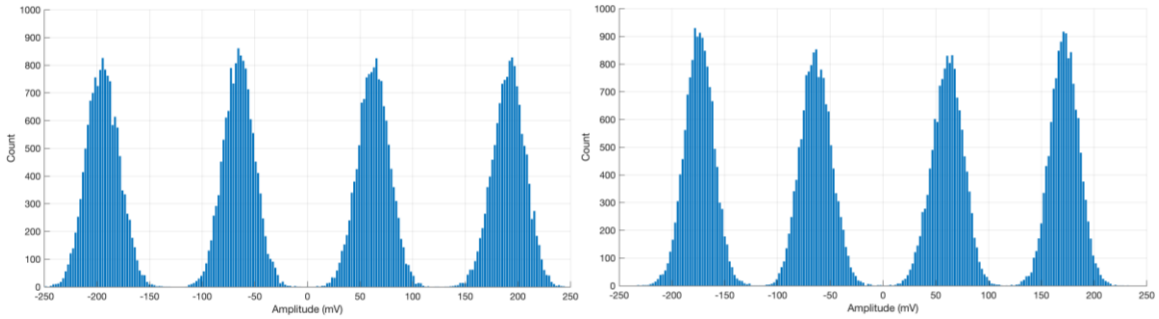


Figure 9. Impact of non-linearity on sample histograms

While the proposed modeling framework supports a wide range of COM-like TX and RX parameters, the simulations are performed in the time domain, directly accounting for non-linear and time-varying effects, resulting in a significant improvement in accuracy compared to COM, in which these are lumped in a single bucket called implementation penalty. System integrators can use the proposed modeling methodology to analyze the performance margin and tradeoffs for different system level design parameters, a task that is currently done, with limited success, through the COM modeling framework.

Using a generic high-level modeling environment (Simulink) to build up top-level models and test-benches enables exploration of a wide range of link configurations, including opto-electrical systems, and evaluation of the interaction between SerDes and FEC. This interaction is typically beyond the coverage of conventional SI simulations.

## 7. Conclusion

In this paper, we first reviewed the common practice of maintaining multiple system models to support the various phases of SerDes IP development, as well as the external modeling collaterals, and the challenges associated with this practice. Then, we outlined three enablers to unify these multiple models into a single modeling framework: object-oriented modeling, fixed-time-step implementation, and automated model export to low-level languages. We followed these enabling guidelines to build a unified parametric ADC-based SerDes model suitable for supporting all internal modeling needs. This parametric model further allows us to augment the external modeling collaterals in order to fill the void between COM and IBIS-AMI models. Next, we correlated the proposed parametric model with a 112 Gb/s SerDes operating over a 39 dB channel. The proposed SerDes modeling framework enables system integrators to achieve a better system observability, well beyond typical SI simulations, while maintaining a high level of model configurability, comparable to COM. This observability and configurability allows for a more efficient exploration of the system performance margins, and ultimately is able to drive co-optimization between the SerDes and the channel designs for leading-edge serial link systems.

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