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IBIS-AMI Modeling and Correlation Methodology for ADC-Based SerDes Beyond 100 Gb/s

Aleksey Tyshchenko, SeriaLink Systems
Clinton Walker, Alphawave IP

David Halupka (SeriaLink Systems)
Richard Allred, Tripp Worrel, Barry Katz (MathWorks)
Adrien Auge (Alphawave IP)

SPEAKERS

Aleksey Tyshchenko

Founder, SeriaLink Systems
aleksey@serialinksystems.com | www.serialinksystems.com

SeriaLink Systems is working on building a configurable modeling flow to support SerDes projects through their entire life cycle: from architecture definition, through analog and digital design, to design validation. Aleksey has been working on behavioral modeling of high-speed SerDes systems, architecture analysis, adaptation, and signal integrity with multi-standard SerDes IP teams at V Semi and Intel.

Clinton Walker

VP of Marketing, Alphawave IP
clint.walker@awaveip.com | www.awaveip.com

Clint has over 24 years of semiconductor and high-speed system design experience. His current role at Alphawave IP is defining technical specifications and IP roadmap for the world's most advanced multi-standard SerDes. Before joining Alphawave IP, Clint was a Senior Director of Analog Mixed Signal IP and Principal Engineer at Intel and spent 22 years driving next-generation standards and technology in the area of high-speed analog IP. Clint was the USB3.0 Electrical Work Group chair and frequently presented for PCIe SIG at developer conferences around the world.

Outline

- **Motivation**
- **ADC-Based IBIS-AMI Modeling Challenges**
- **ADC-Based IBIS-AMI Modeling Methodologies**
  - COM-Representative ADC-Based Models
  - Architecturally-Representative ADC-Based Models
  - Maximum Likelihood Sequence Estimation (MLSE) Models
- **SNR-Centric Model Correlation Methodology**
- **Conclusion**

Motivation

- Data rates in serial link systems keep growing, reaching 100 Gb/s and beyond
- Channel losses and higher-order modulation (PAM4) necessitate more extensive equalization
- ADC-based SerDes architectures are becoming prevalent
- Equalization is divided between analog and digital domains
- This allows for extensive digital equalization that scales well with process nodes
- Digital equalization leads to a deviation from conventional (non-ADC-based) SerDes
- IBIS-AMI models remain de-facto technical link between SerDes vendors and system integrators
- IBIS-AMI modeling relies on conventional (non-ADC-based) architectural assumptions
- Architectural misalignments make it challenging to build IBIS-AMI models for ADC-based SerDes
- What are these challenges? What are possible ways to address these challenges?

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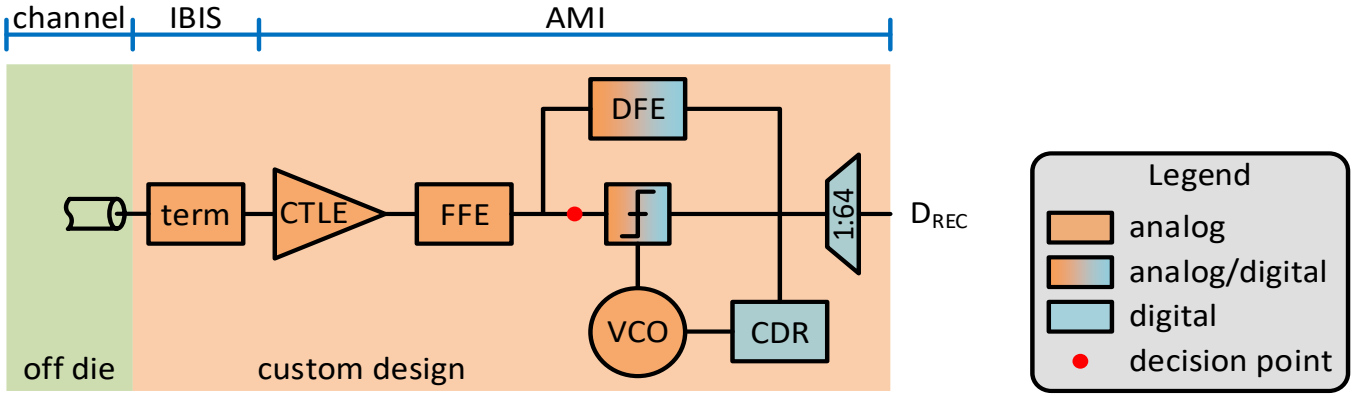
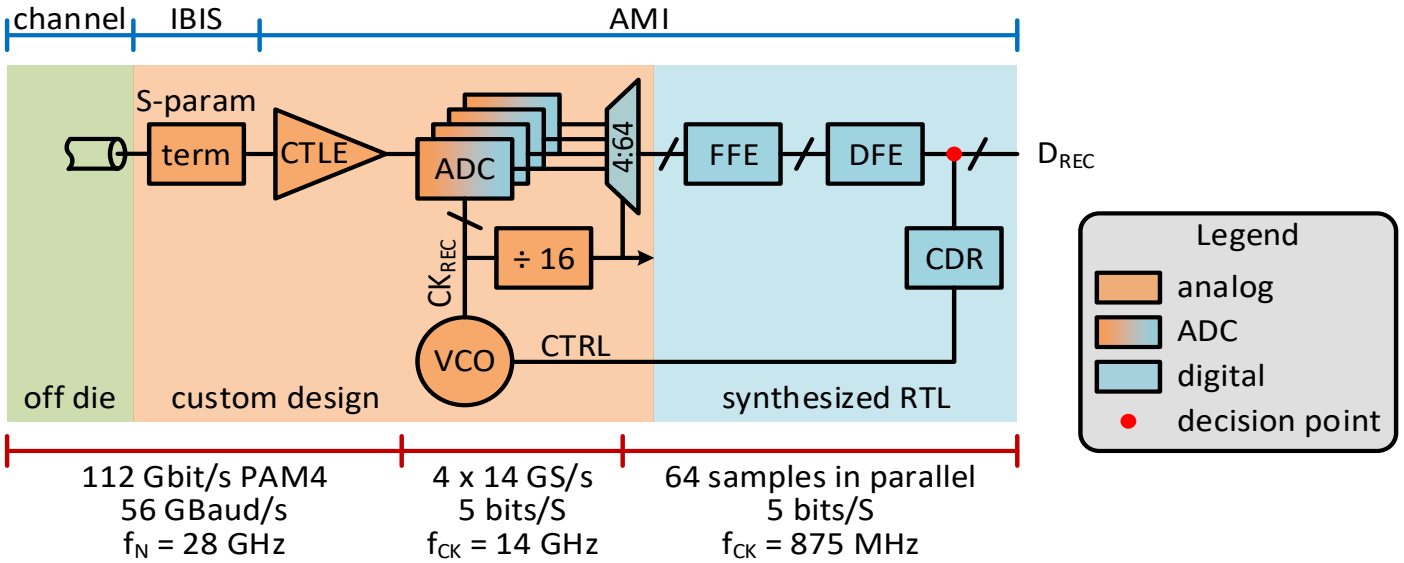
IBIS-AMI Framework



- Decouple model from simulator by standardizing the interface
- Decision point: equalized analog waveform at M samples per UI
- Simulator evaluates link margin in statistical and time domains
- Sampler performance is communicated through margin/eye mask requirements
- Simulator accounts for additional noise and jitter sources

ADC-Based SerDes Topology



- Time-interleaved (multi-path) ADC takes 1 sample per UI and de-muxes samples
- Mueller-Müller baud-rate CDR recovers clock from equalized ADC samples
- FFE, DFE, CDR are all in a DSP block that operates on de-muxed data, 0.5-1.0 GHz
- This does not fit well into IBIS AMI framework

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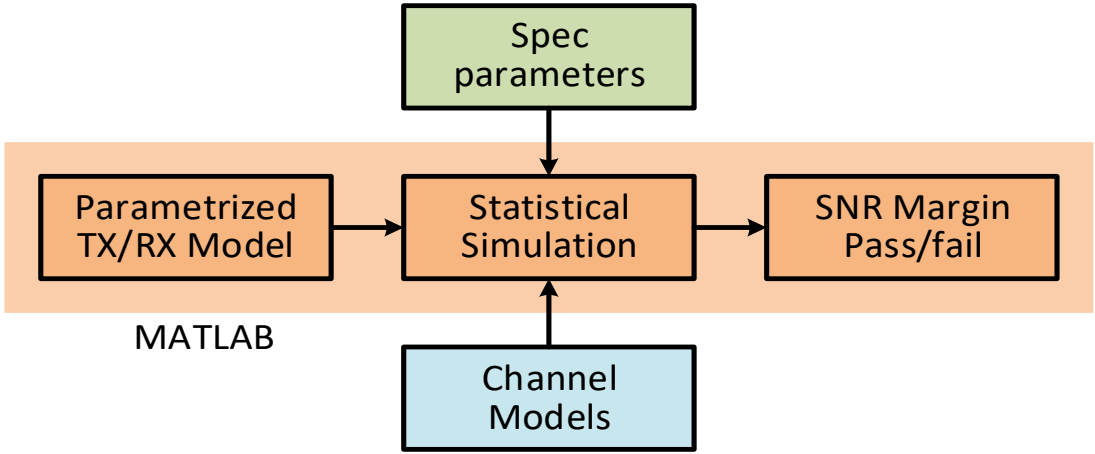
COM as SerDes Definition Tool



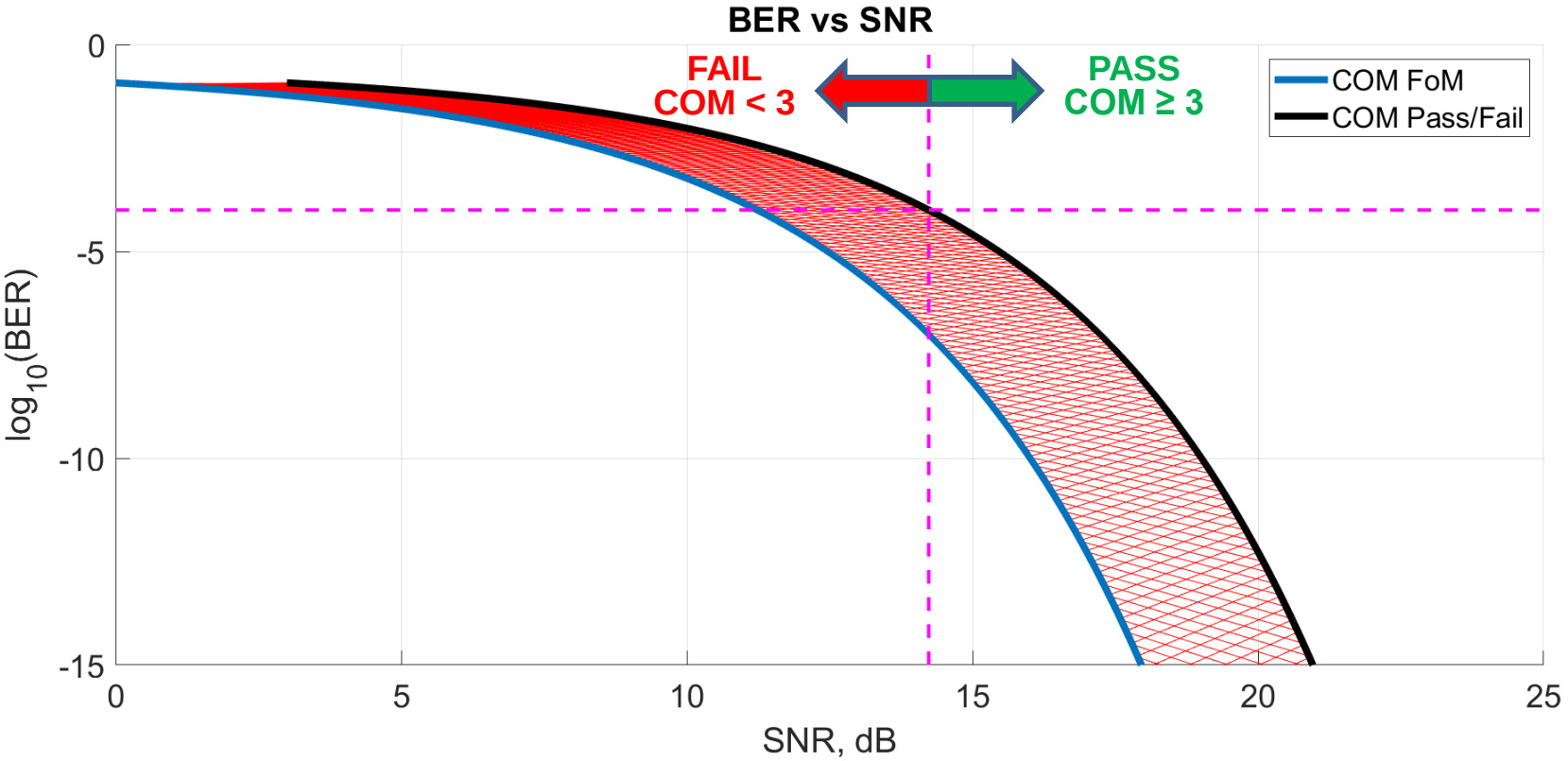
PROS

- Vetted by a large number of experts
- Generic parametrized model
- Spec details come from spreadsheet
- Runs in MATLAB, code is available
- Quick simulation iterations

CONS

- Lacks ADC, non-linearities
- Lacks clock recovery details
- Non-expandable for detailed modeling
- No time domain effects captured
- Intended for analog architectures

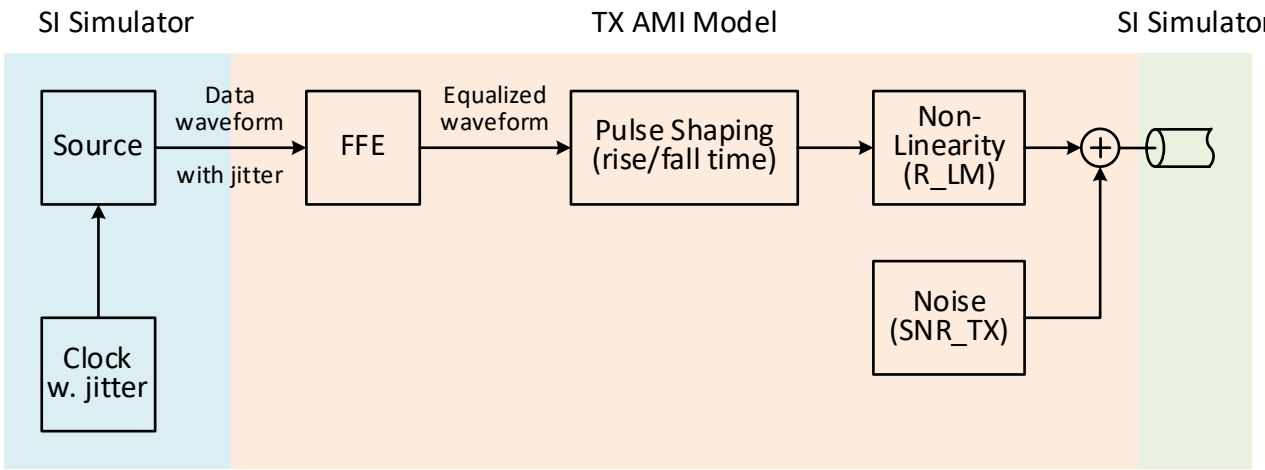
COM Implementation Margin



COM and ADC-based SerDes Architectures

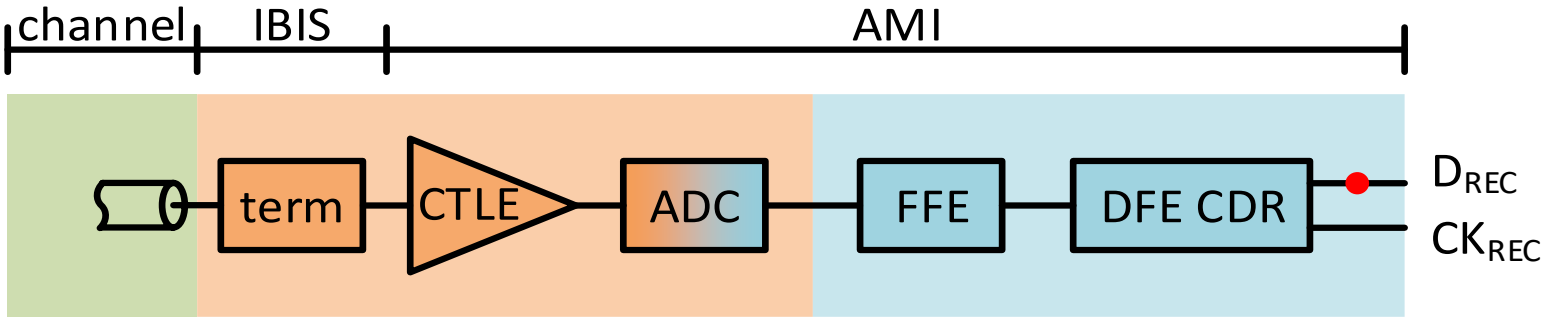
- Similar to IBIS-AMI, COM was intended for conventional analog-centric SerDes architectures
- COM uses a fully-equalized pulse response as a starting point for SNR analysis
- Some non-linear and time-varying (non-LTI) effects are accounted for as SNR penalty
- However, COM abstracts away SerDes implementation details
- COM focuses on equalization performance of the reference SerDes model
- Digital FFE and DFE are approximated as a full-rate equalizers
- As a result, a fully-equalized pulse response is available in COM
- ADC-related performance penalty is covered by the implementation margin
- Can we build ADC-based IBIS-AMI models using a similar approach?
- Can we add ADC performance penalty explicitly in time domain simulations?

TX Model Block Diagram



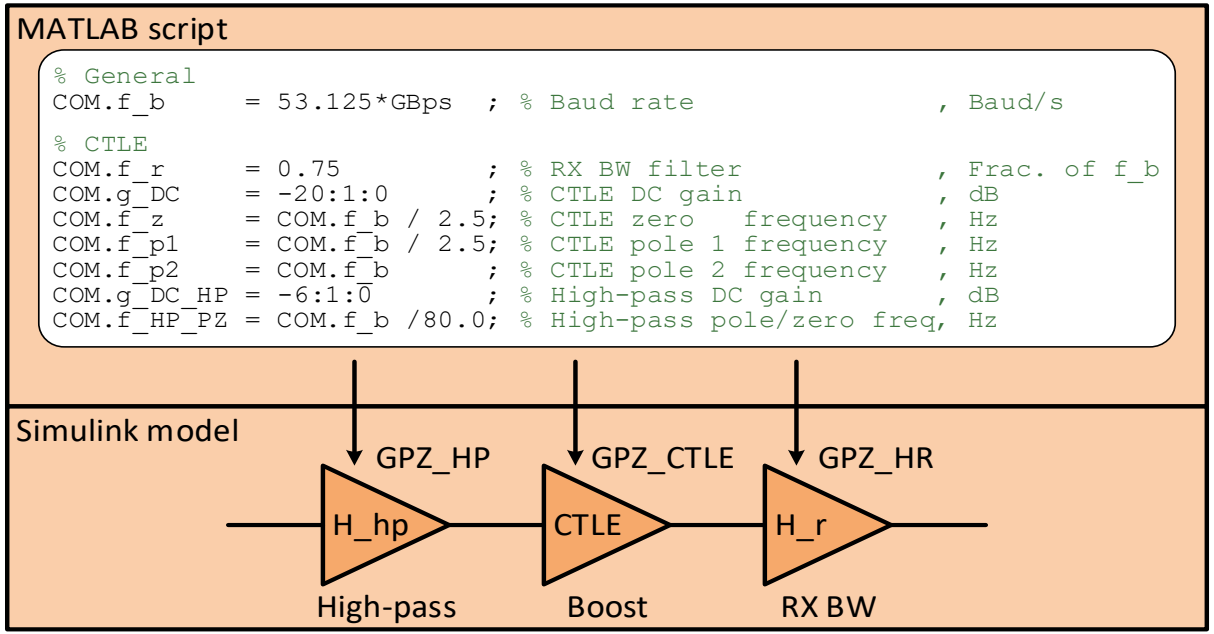
- Includes same components as COM reference TX, supports statistical and time domain simulations
- COM-parametric IBIS-AMI TX model with two intended use cases
  - Can be configured to represent a standard-compliant TX
  - Can be configured to represent measured TX performance

COM-Representative ADC-Based RX Model



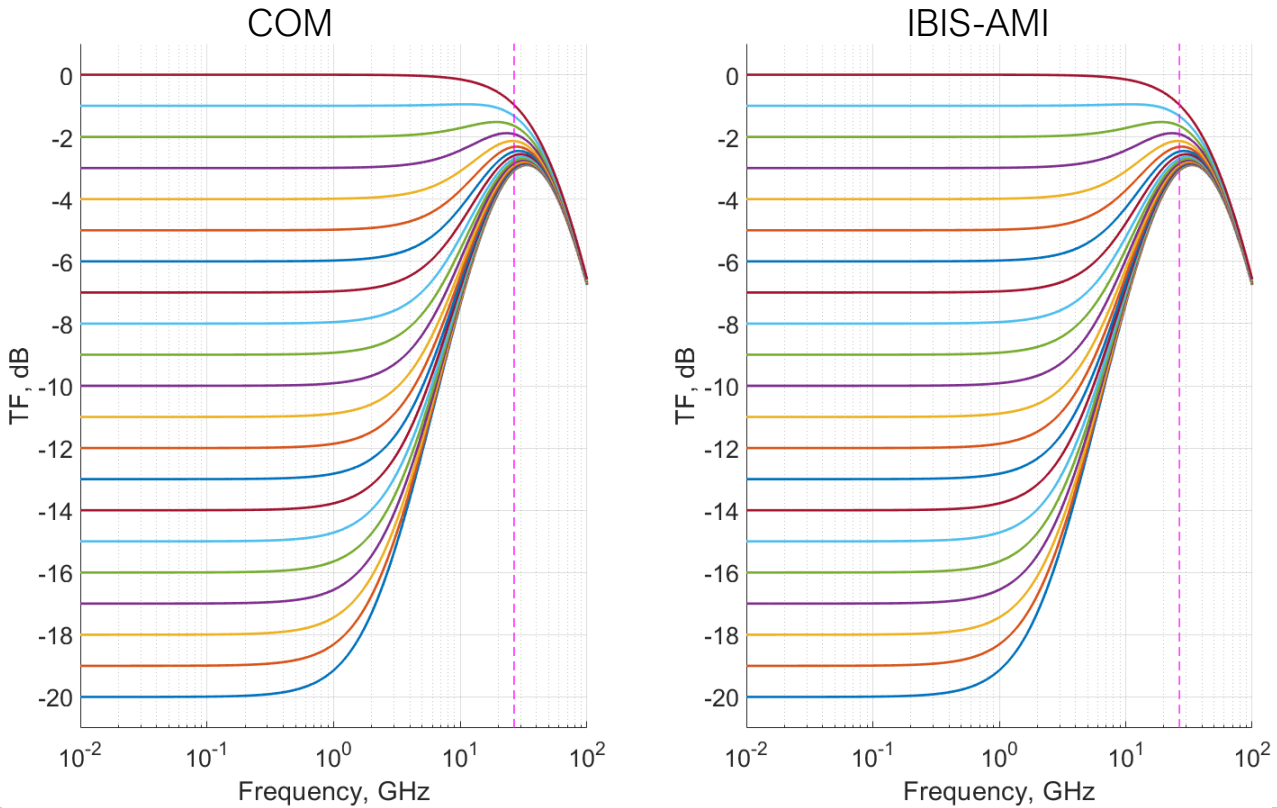
- Statistical
  - Recover clock phase from pulse response with MM CDR
  - Adapt equalization: CTLE, FFE, DFE
  - Re-adjust recovered clock phase after adaptation
- Time domain
  - ADC is a time-agnostic quantizer
  - Mueller-Müller CDR runs continuously, maintains phase lock
  - Equalization parameters are constant during transient simulation

CTLE Configuration



- A script converts COM CTLE definition into GPZ matrices for CTLE stages
- Automatically update block properties in Simulink and range of AMI parameters
- In a similar way, CTLE can be configured to represent actual circuit performance

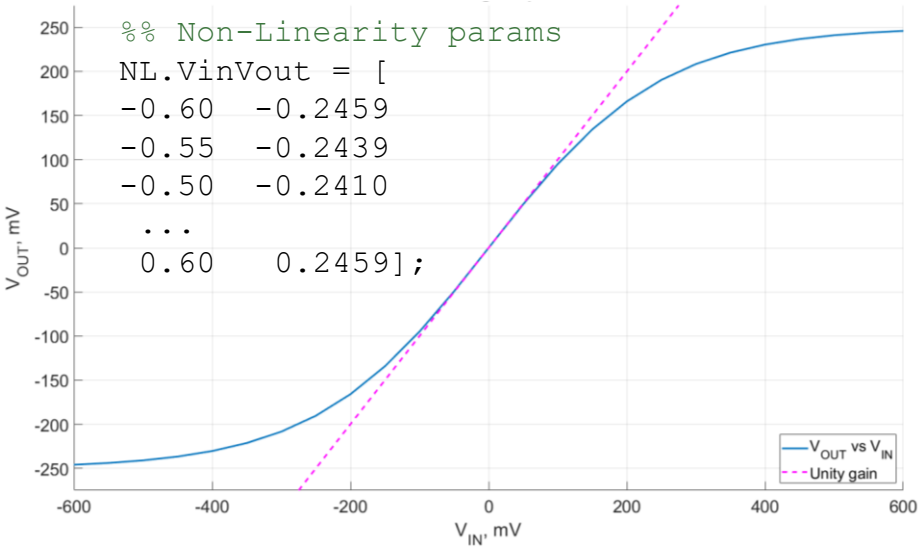
CTLE Set of Transfer Functions



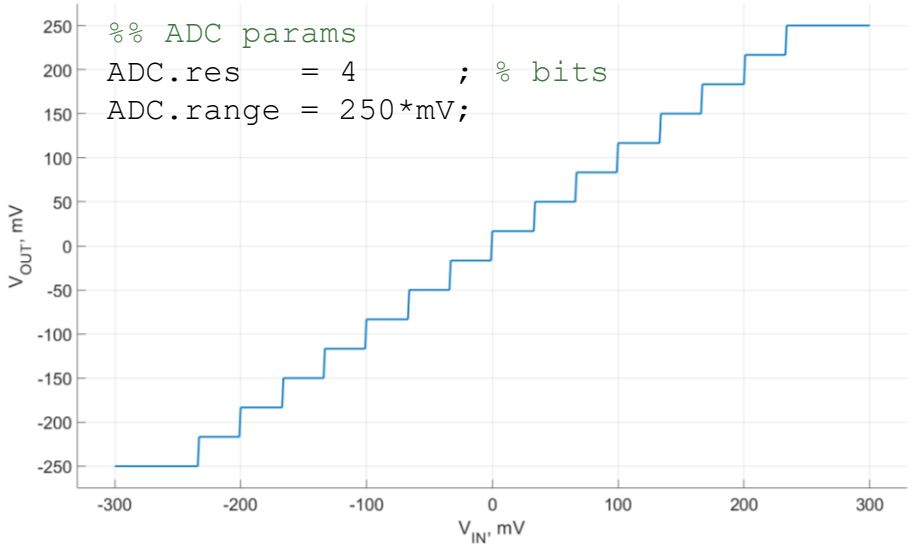

```
%% COM parameters
COM.f_b  = 53.125*GBps    ;
COM.g_DC = -20:1:0        ;
COM.f_z  = COM.f_b / 2.5  ;
COM.f_p1 = COM.f_b / 2.5  ;
COM.f_p2 = COM.f_b        ;
```

Non-Linearity and ADC

```
%% Non-Linearity params
NL.VinVout = [
-0.60   -0.2459
-0.55   -0.2439
-0.50   -0.2410
  ...
 0.60    0.2459];
```

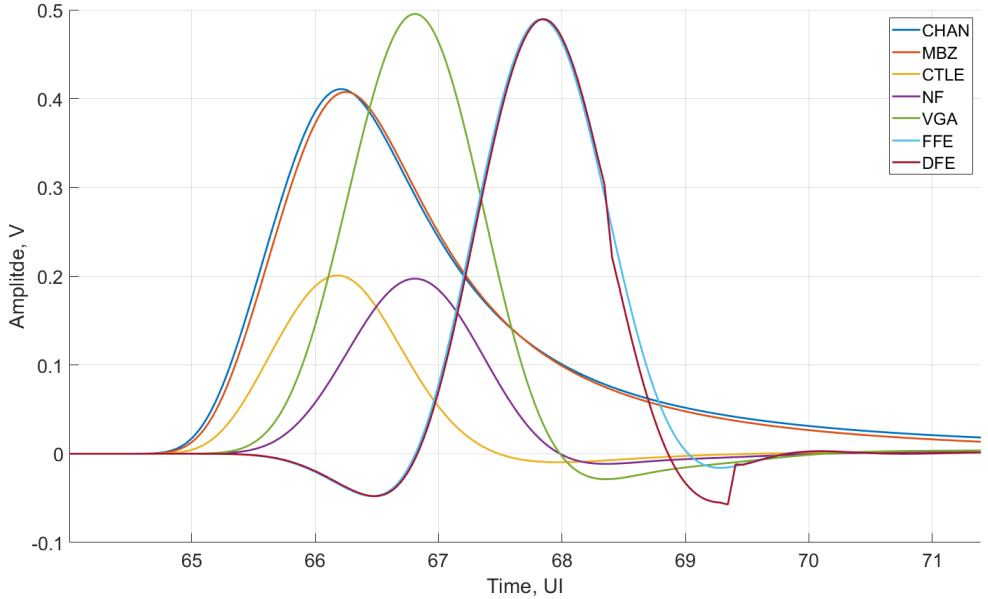



```
%% ADC params
ADC.res    = 4      ; % bits
ADC.range = 250*mV;
```



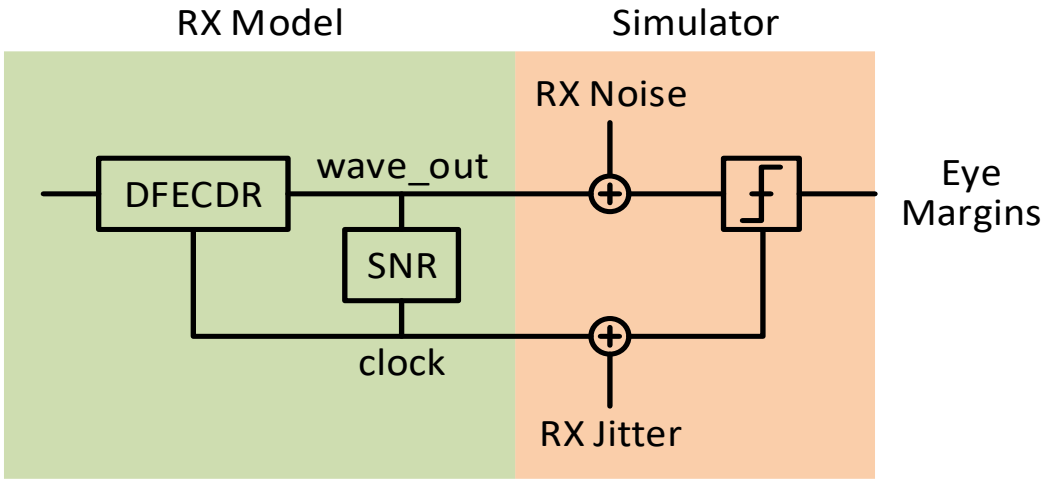
- Non-linearity is added to the data path between CTLE and ADC
- ADC is a quantizer, need voltage (not bits) at output to play well with IBIS AMI flow
- Resolution and dynamic range are the ADC parameters

Adaptation in Statistical Domain



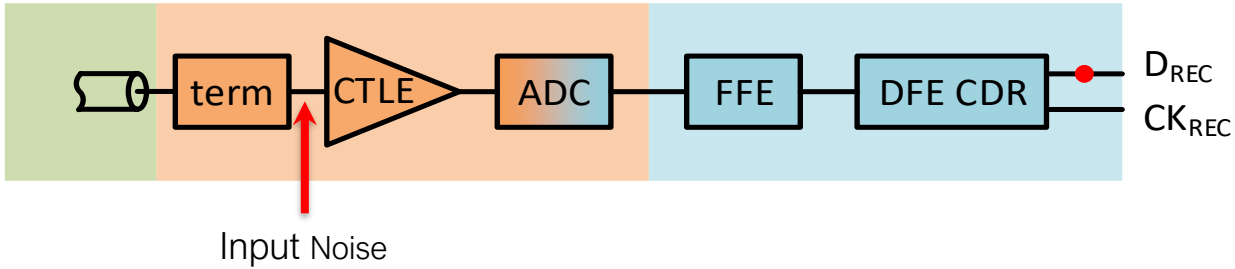
- Use equalized pulse response to guide the adaptation
- Using Mueller-Müller phase detection for FFE & DFE zero-forcing
- FFE is “aware” of DFE: FFE brings Tap 1 to be within DFE range, similar to COM

RX Noise Impact on SNR



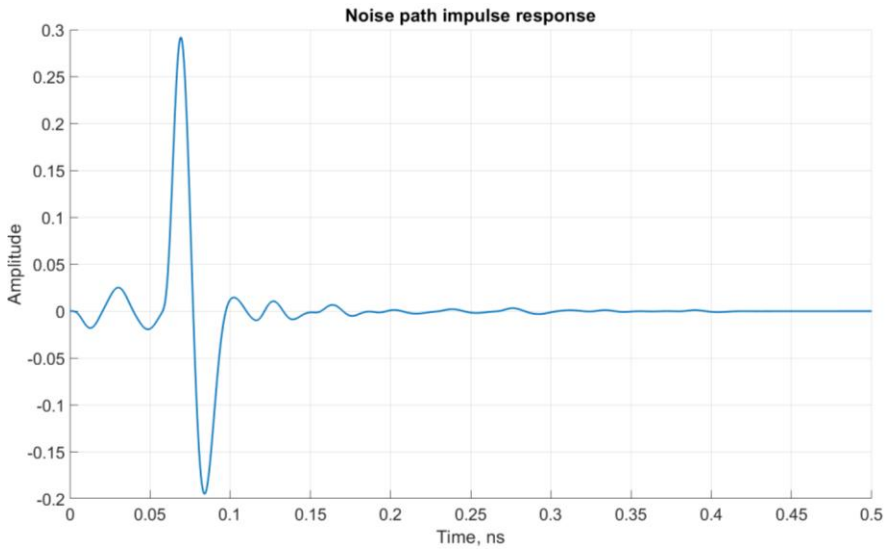
- RX noise and jitter can be added by the simulator to RX model outputs
- This impacts eye margins calculated by the simulator
- However, RX noise is not visible to SNR monitor inside RX
- We would like to account for output-referred noise for adaptation and correlation
- Therefore, input-referred noise needs to be added to the model

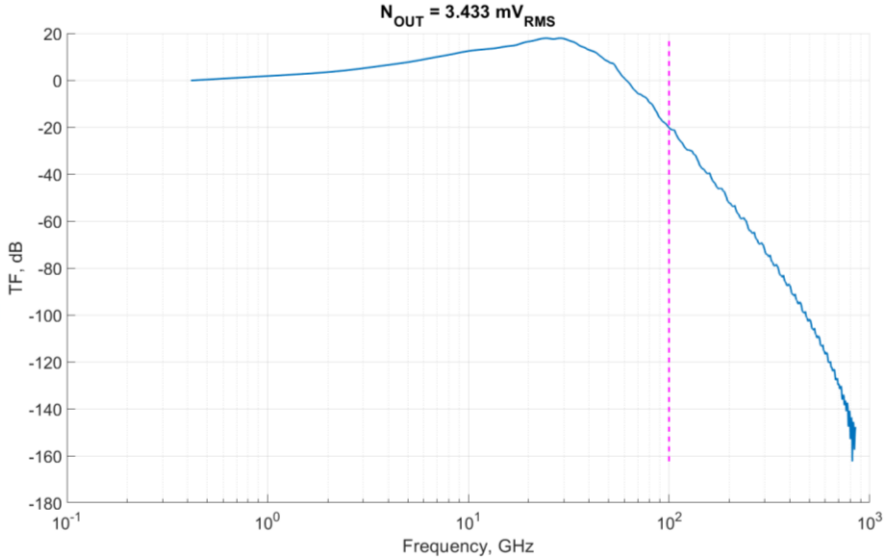
RX Noise in Statistical Adaptation



- Input noise
  - White noise up to simulation BW
  - Noise PSD is a parameter in COM spreadsheet, eta_0
- Output noise
  - Apply linear EQ to filter noise
  - Integrate filtered noise in frequency to get RMS value
  - Output RMS noise degrades adaptation FoM (SNR)
- However…
  - Adaptation is done in statistical part of the model
  - Statistical domain is intended for impulse processing
  - Need to get output noise PSD using only impulse processing

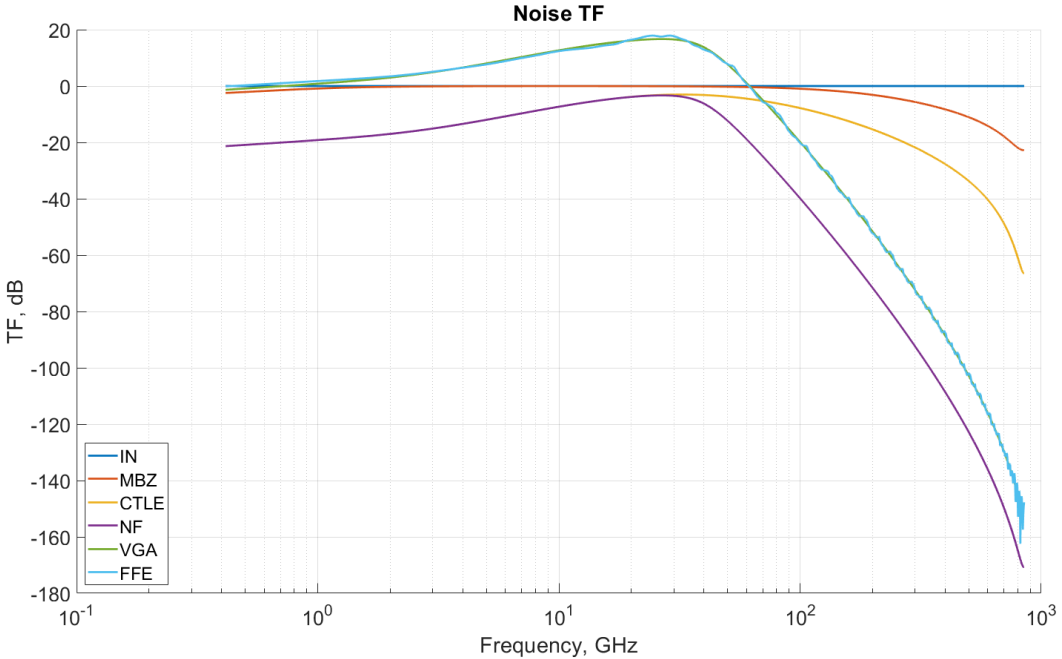
RX Noise in Statistical Adaptation





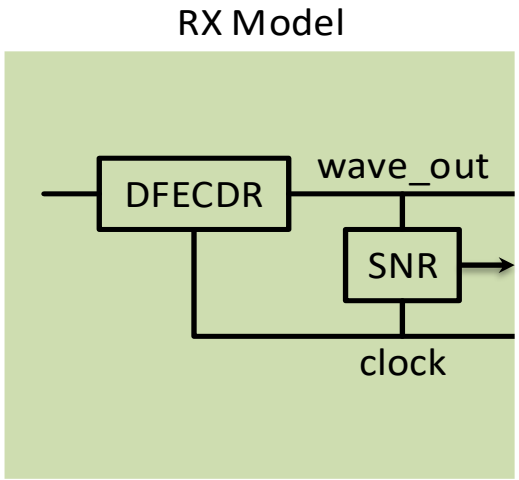
- Use a unity impulse to “probe” response of linear EQ blocks: CTLE, VGA, FFE
- FFT to convert noise path IR to frequency domain
- Scale noise TF by input PSD, integrate up to 100 GHz to get output noise RMS
- This noise methodology correlates well with COM and time domain simulations

RX Noise in Statistical Adaptation



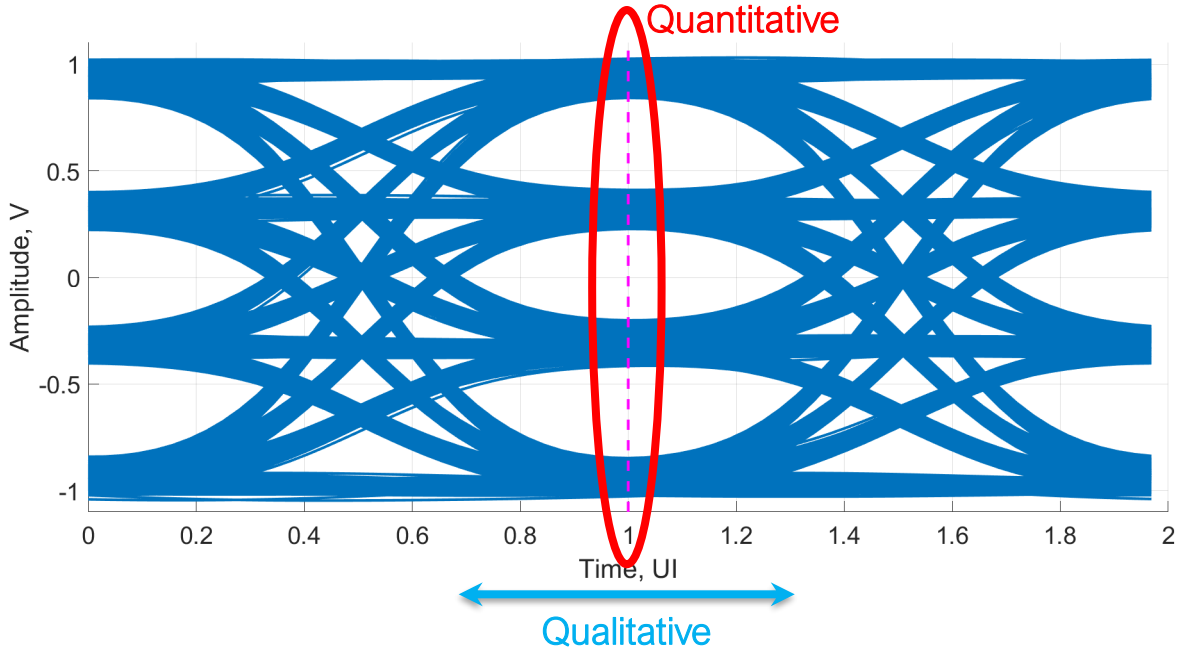
- Converting noise path IR to frequency domain after every equalization stage
- This illustrates noise shaping progression through the RX

SNR Measurement Block



- Measures SNR at UI centers, supports NRZ and PAM4
- Drives adaptation in statistical domain; correlation parameter with COM in time domain
- Used for post-Si SNR correlation with SerDes IP

Eye Diagram in COM-Representative Models



- Since ADC is modeled as a blind oversampling quantizer, the eye diagram is available (similar to COM)
- Only vertical eye opening (amplitude histogram) at the sampling instance carries quantitative information
- Horizontal eye opening (time histogram) carried only qualitative information in this eye diagram

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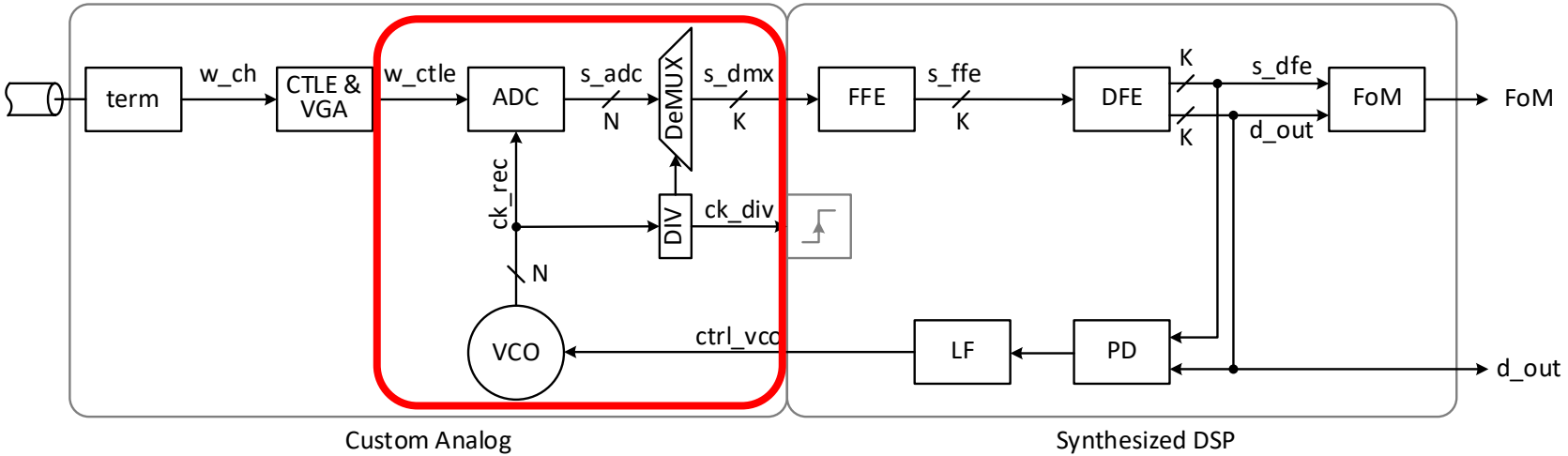
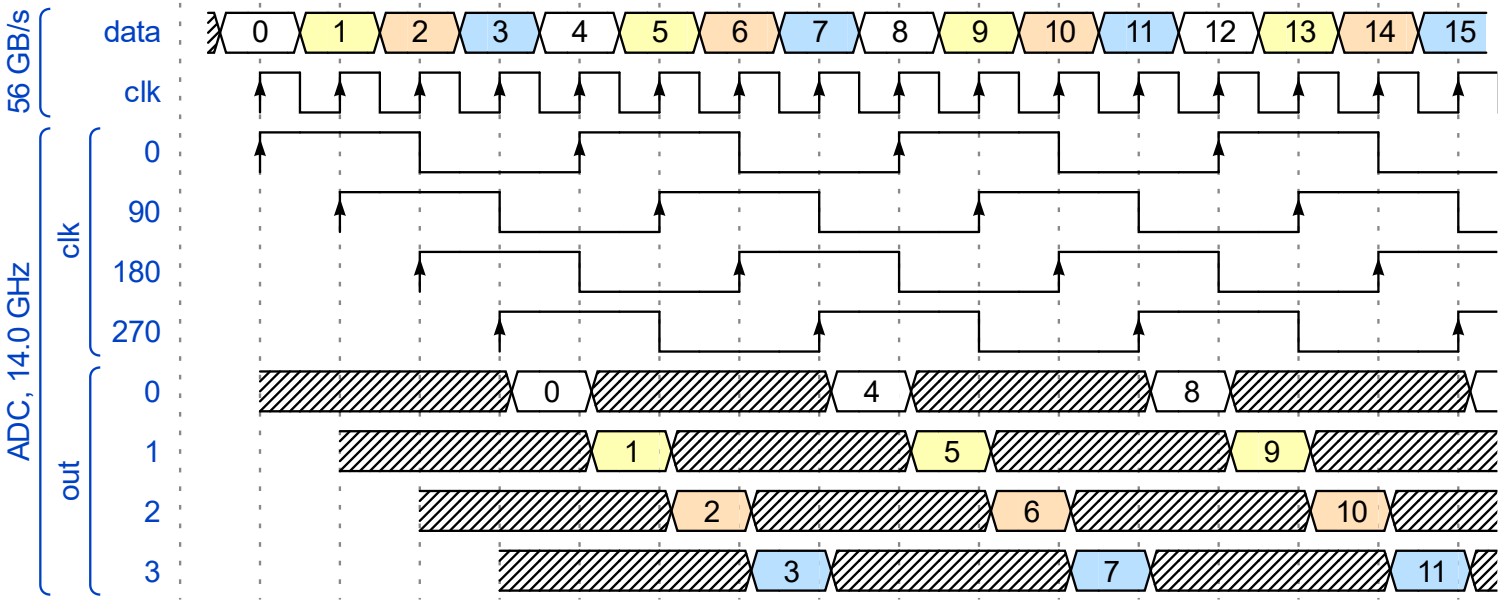
ADC-based RX Block Diagram



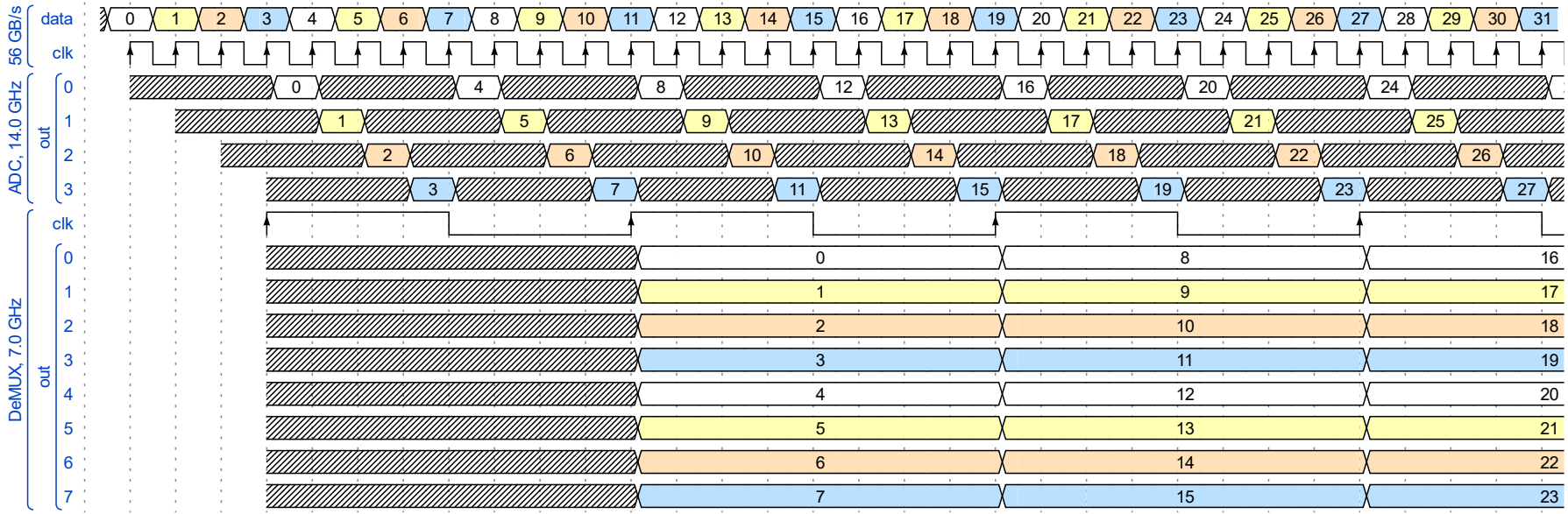
- Analog equalization, CTLE & VGA, operates on continuous-time waveform
- Digital equalization, FFE & DFE, operates on discrete-time samples at UI centers
- Partially-equalized analog waveform needs to be sampled in time, and converted to digital representation
- For practical DSP implementation, it operates on frames of parallel samples at a lower frequency

ADC Time Interleaving Depth



- *N* time-interleaved ADCs sample at the rate of 1/*N* each, requiring *N*-phase recovered clock
- ADC samples capture information at UI centers, discard the rest of the waveform information
- Time interleaving depth trades off ADC operating speed with circuit and clocking complexity

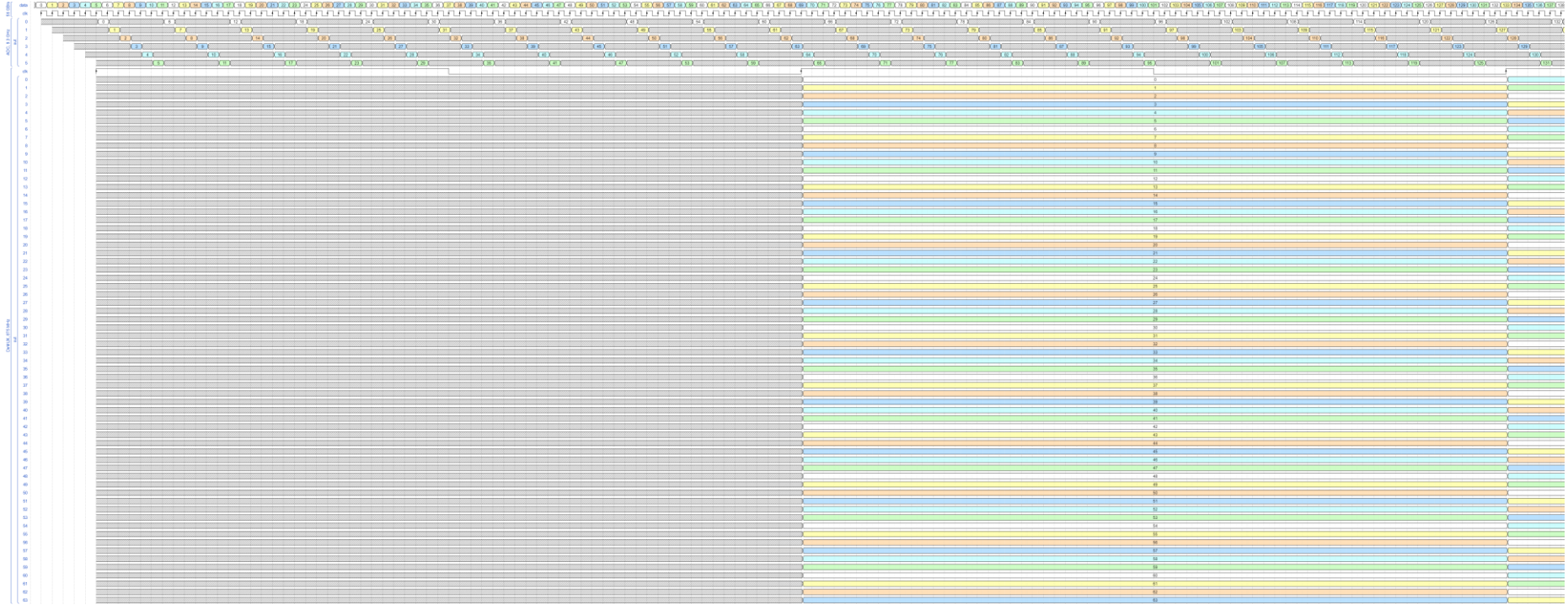
Sample Demultiplexing: 4:8 Ratio



- *N* samples at ADC output are demultiplexed into frames of *K* parallel samples
- Digital equalization in DSP operates on sample frames at the rate of 1/*K* with respect to baud rate
- Demultiplexing trades off DSP operating speed with data path latency, and clock recovery dynamics

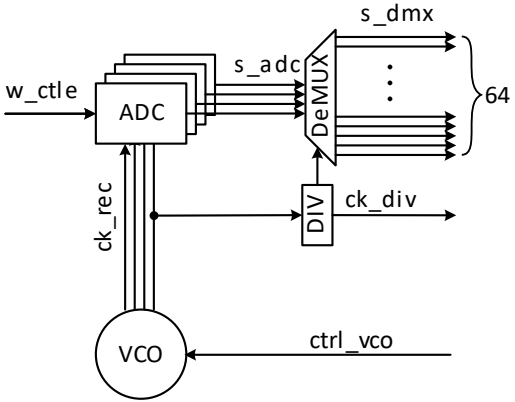
Sample Demultiplexing: 6:64 Ratio, 875 MHz Output

Latency = 100 UIs = 1.8 ns

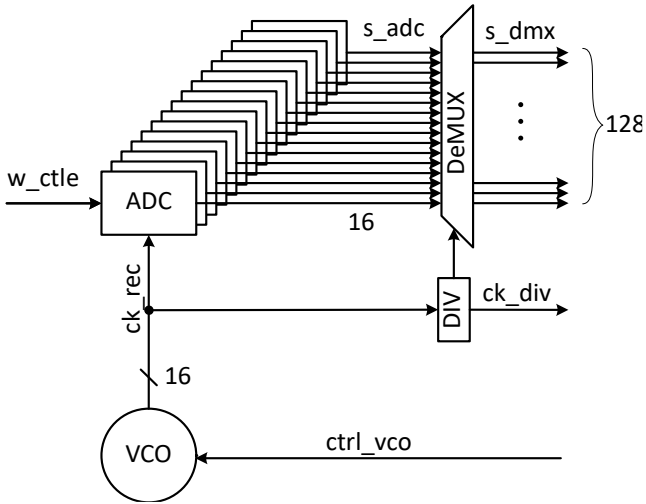


ADC-Based RX Block Interfaces

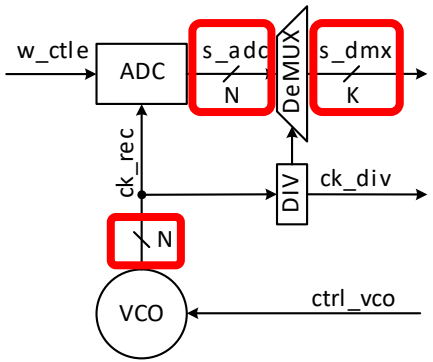
4-way time-interleaved ADC
64-sample DSP frame



16-way time-interleaved ADC
128-sample DSP frame

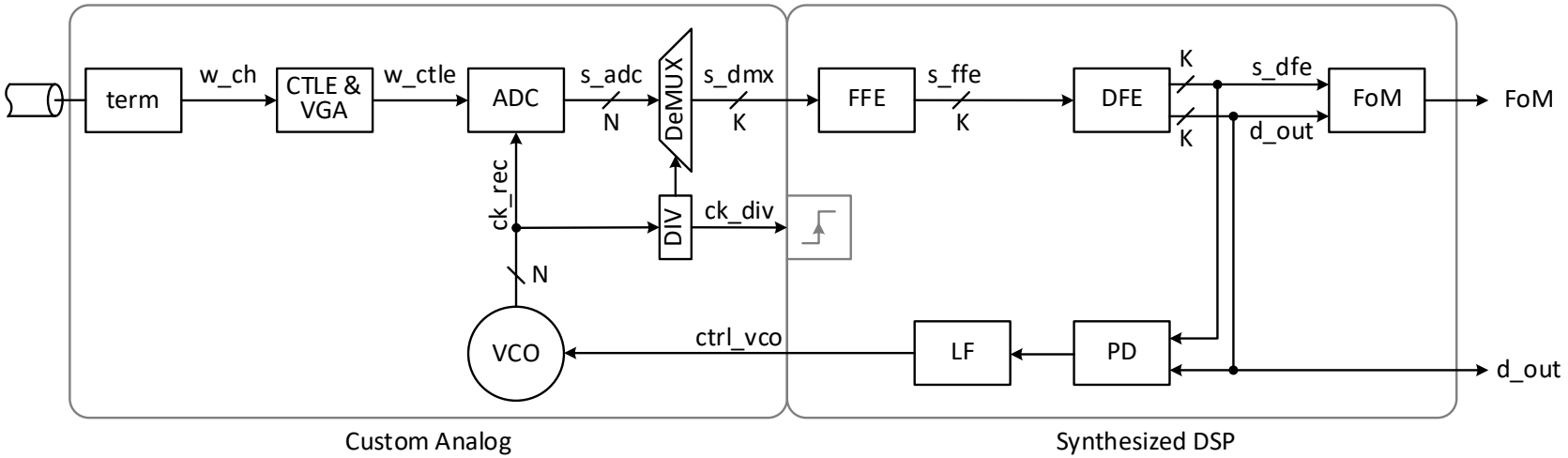


Parametric



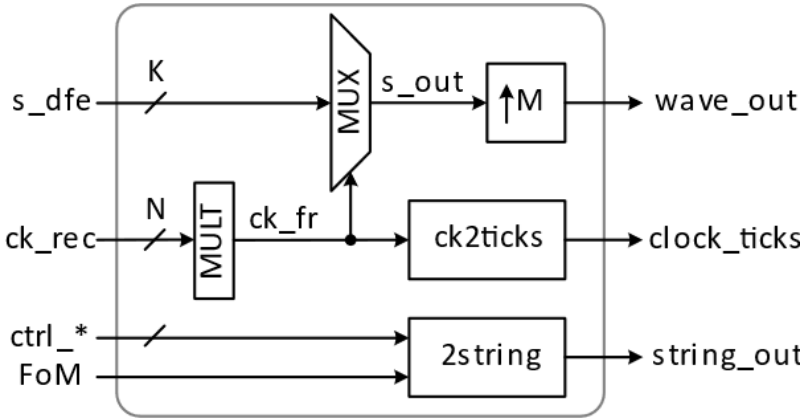
- Parallel processing adds complexity to Simulink models
- Exploring key design parameters is difficult in Simulink
- Proposed model enables low-effort parametric design-space exploration

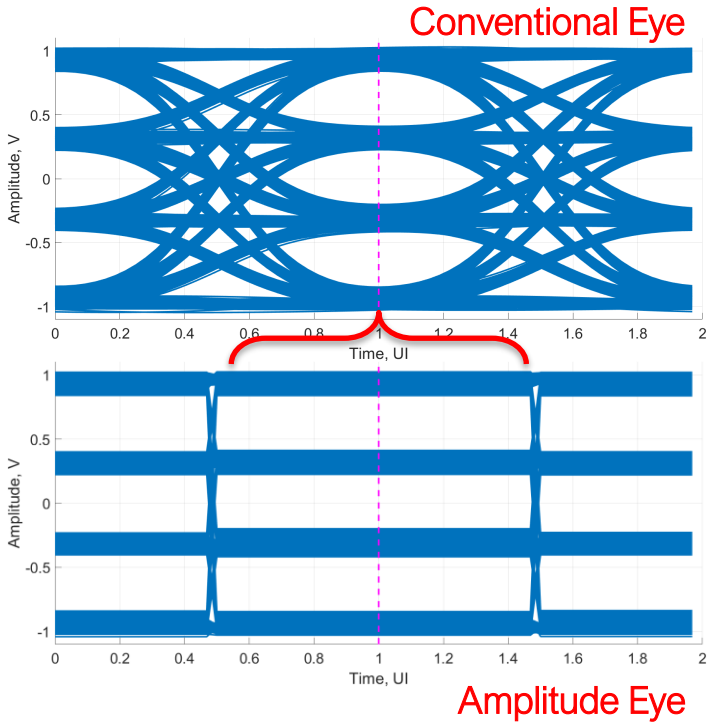
IBIS-AMI Interface with ADC-based RX



- Fully-equalized continuous-time waveform does not exit in ADC-based RX, cannot construct an eye diagram
- Instead, fully-equalized UI-center samples are available, in frames of *K*-samples at 1/*K* rate – *s_dfe*
- Full-rate clock that triggers a samples does not exist either
- Instead, 1/*N* rate *N*-phase clock triggers the ADC at cumulative rate of 1 sample per UI – *ck_rec*
- How to interface this with SI simulators that expect a fully-equalized waveform along with a full-rate clock?

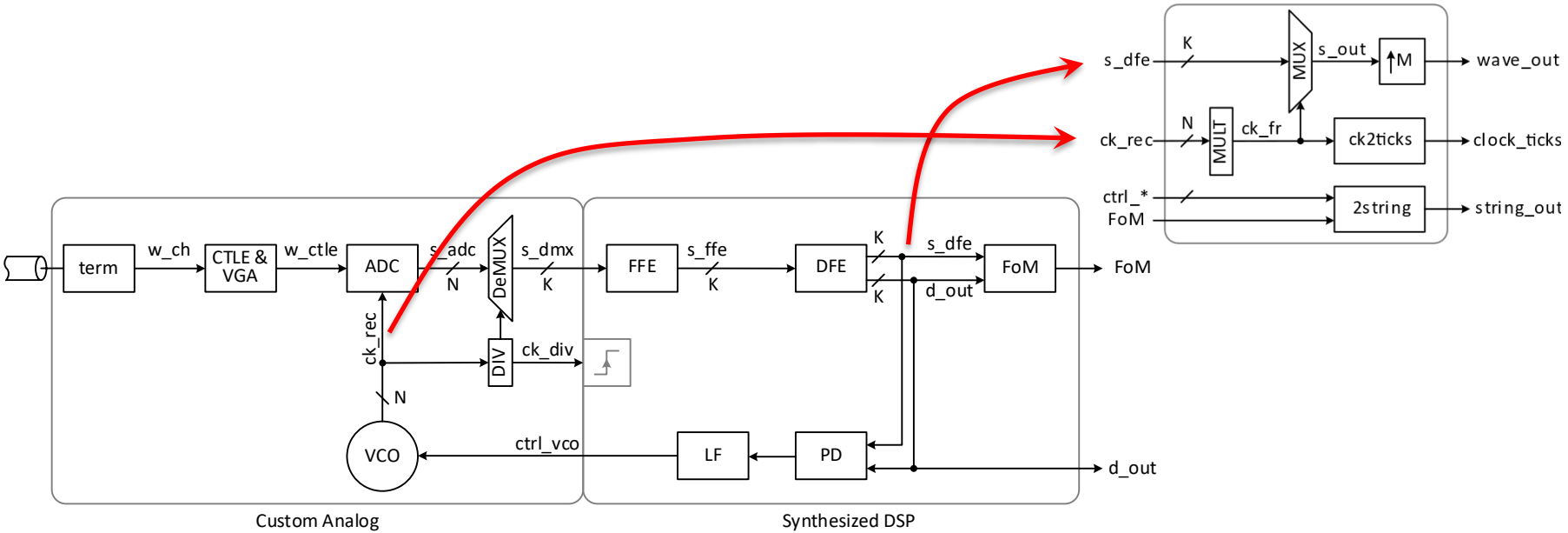
IBIS-AMI Bridge





- Multiplex frames of equalized samples, *s_dfe*, into baud-rate sequential samples, *s_out*, still at 1 S/UI
- Up-sample to required number of samples per UI, *M*; amplitude remains constant within every UI
- Output waveform, *wave_out*, is compatible with IBIS-AMI requirements, but carries no timing information

Architecture-Representative ADC-Based RX Model



- RX model captures all architectural and implementation details without IBIS-AMI constraints
- IBIS-AMI bridge interfaces the detailed RX model with SI simulators
- Only vertical eye opening (amplitude histogram) is available, consistent with ADC-based architectures

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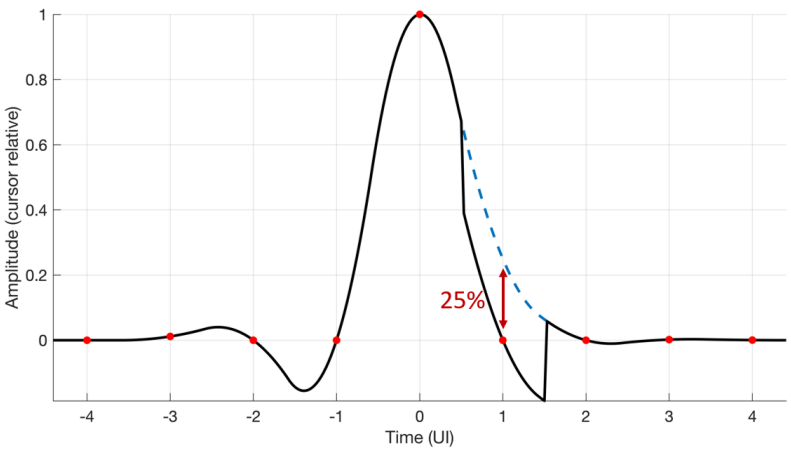
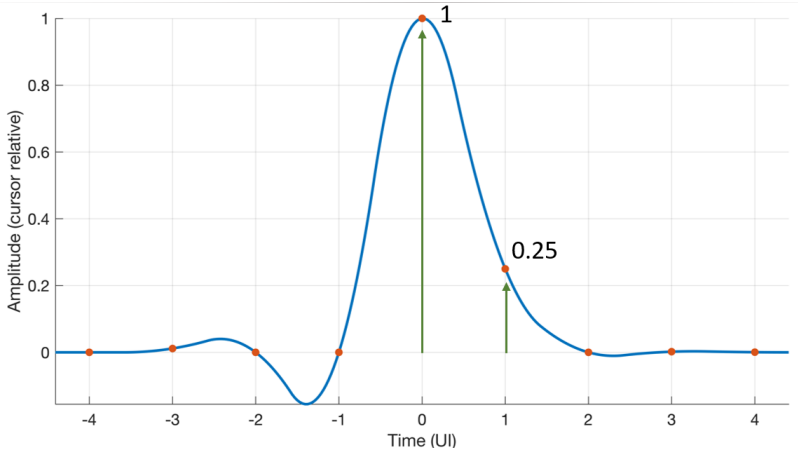
Maximum Likelihood Sequence Estimation



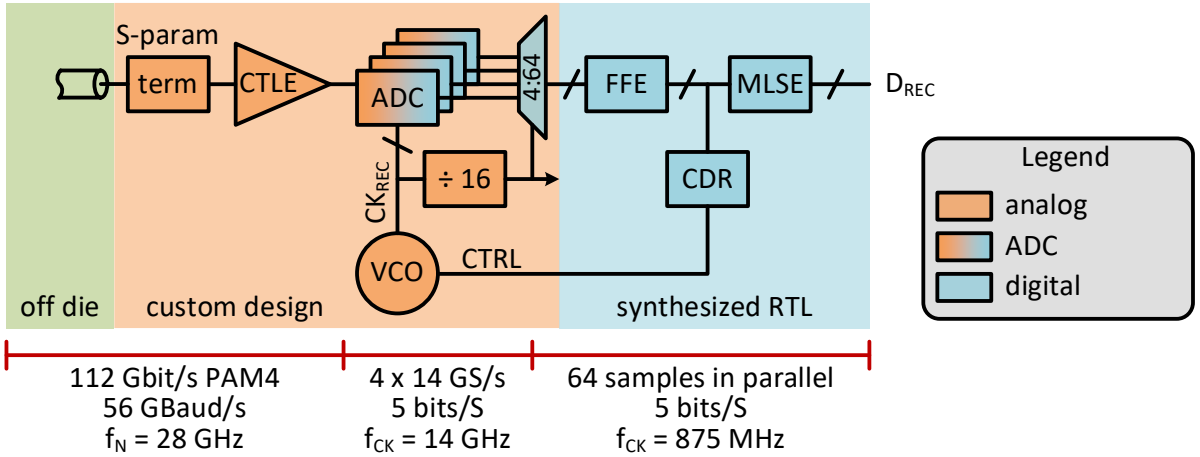
Conventional Equalization



MLSE

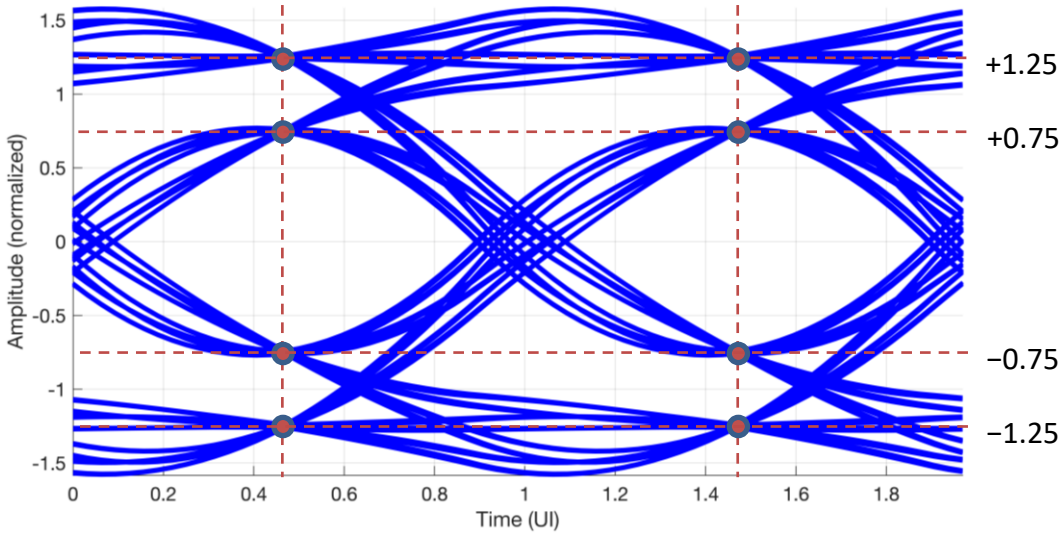
- Conventional equalization cancels ISI, discarding received pulse energy outside the symbol boundaries
- MLSE leverages residual ISI energy to improve SNR and BER
- Pulse at MLSE input needs to contain known (controllable) amount of ISI

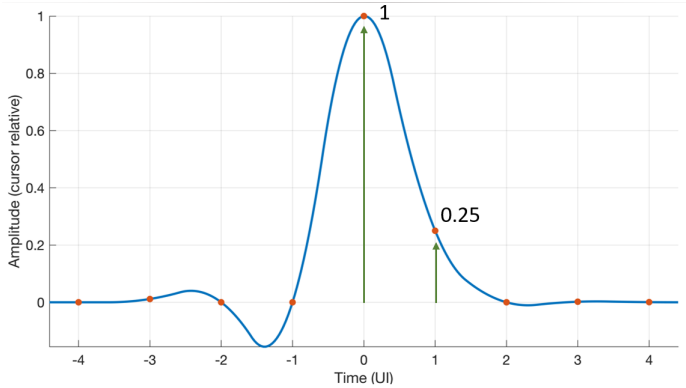
RX with MLSE Block Diagram



- MLSE is a digital algorithm that operates on partially-equalized received samples, outputs data decisions
- FFE is configured to drive equalization towards a target pulse as opposed to zero ISI
- Since MLSE output has no timing or residual ISI (data symbols only), clock recovery loop uses FFE output

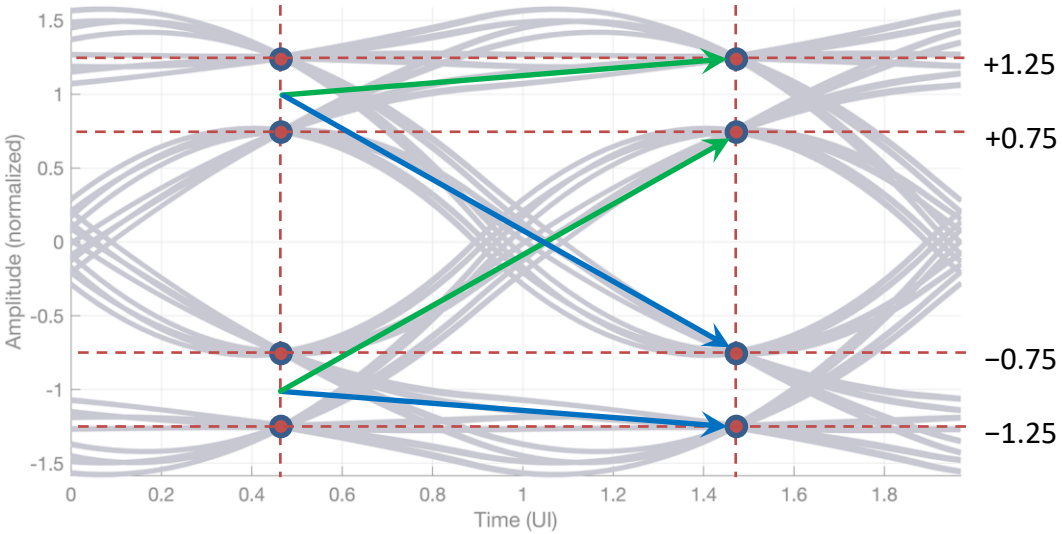
From Pulse to Eye Representation

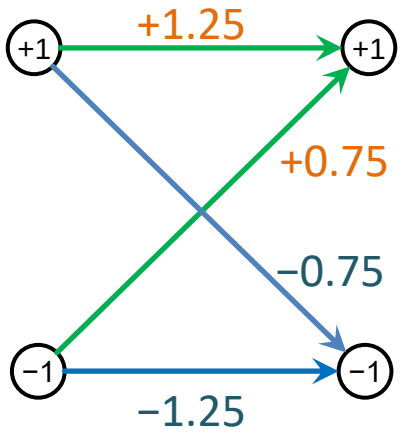




- Significant 1st post-cursor ISI in pulse response leads to level separation in eye diagram
- +1 data symbol corresponds to two levels: +cursor ± post-cursor = +1.00 ± 0.25 amplitudes
- –1 data symbol corresponds to two levels: –cursor ± post-cursor = –1.00 ± 0.25 amplitudes

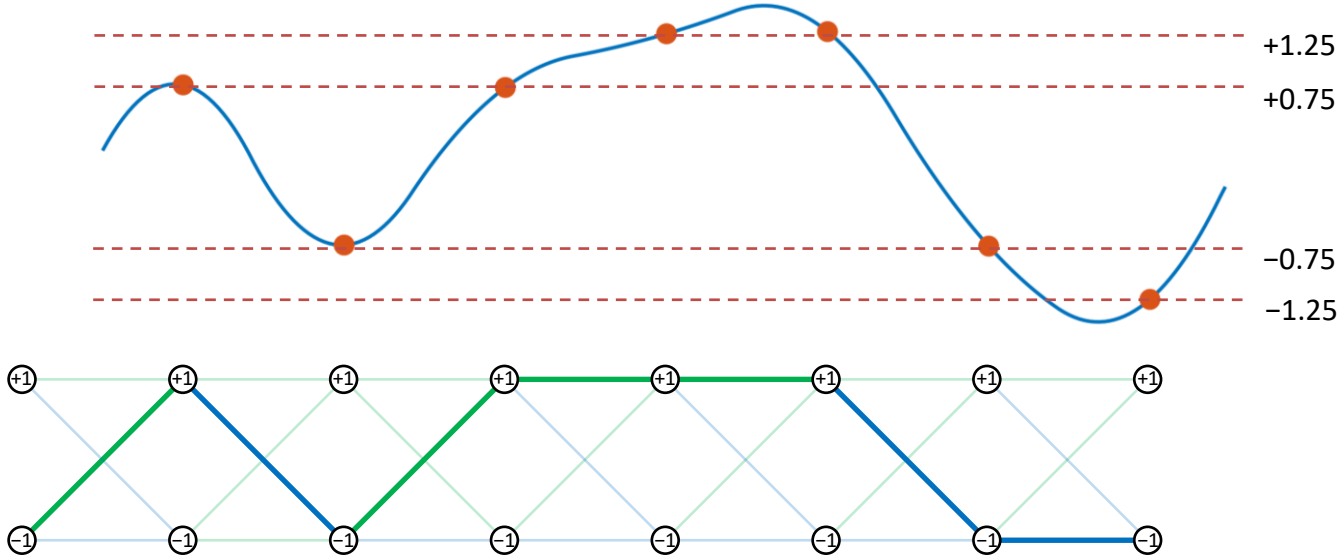
From Eye to Trellis Representation





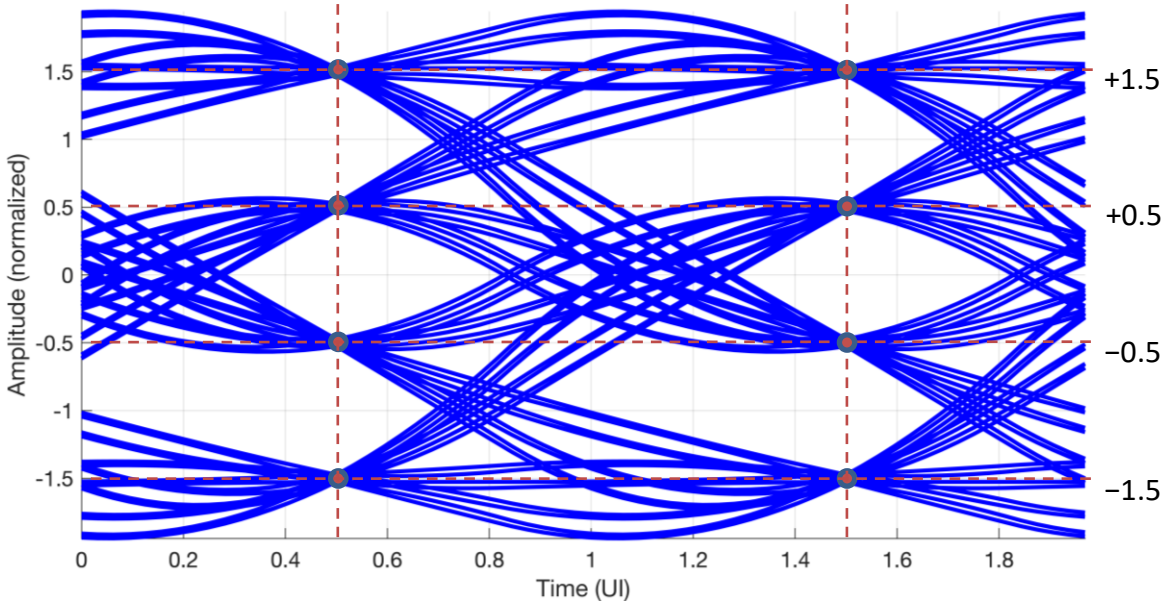
- Eye diagram can be represented as a trellis segment
- Vertices represent data symbols, edges represent transitions between symbols
- Resulting amplitudes are assigned to trellis edges as expected amplitudes at destination nodes

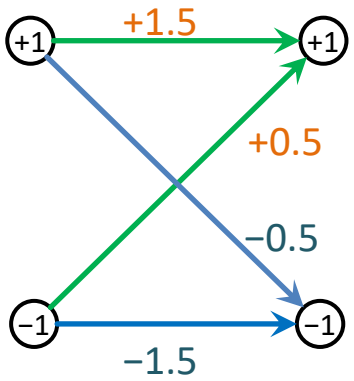
Traverse Trellis for Sequence Estimation



- Partially-equalized waveform (sequence of samples) at FFE output forms a path through a trellis diagram
- Deviation of observed from expected sample amplitudes forms edge cost or penalty
- Trellis path with lowest cost (penalty) corresponds to a data sequence estimate with maximum likelihood
- Algorithms similar to Viterbi are frequently used for trellis traversal

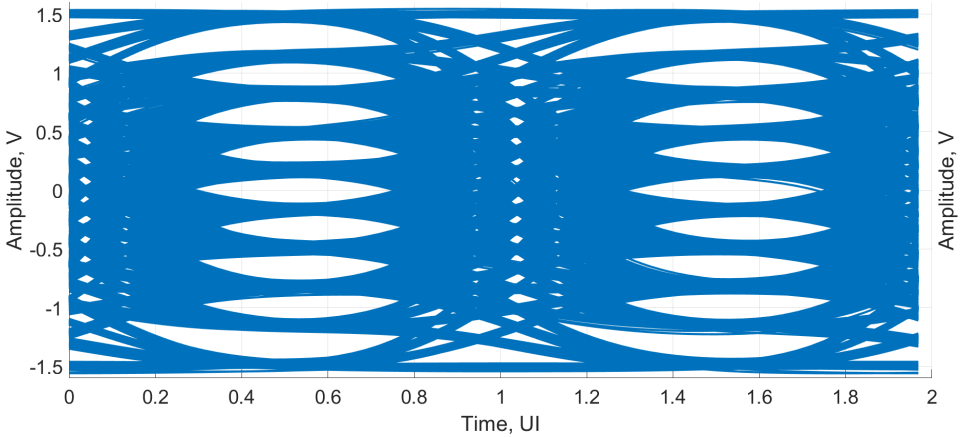
NRZ Eye at MLSE Input with [1.0 0.5] Target Pulse



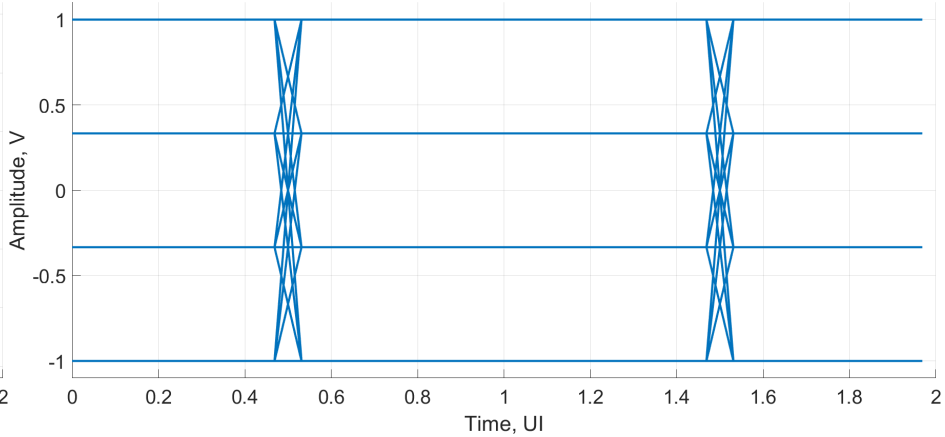


- Larger ISI in target pulse leads to more significant eye closure, this NRZ eye resembles PAM4 eye
- Even in noise-free case, SI simulators are unable to use MLSE input eye for link performance evaluation
- This resemblance with PAM4 illustrates that MLSE allows to operate with lower equalization BW margins

MLSE Eye Diagram



PAM4 Eye at MLSE Input



PAM4 Eye at MLSE Output

- Signal (eye) at MLSE input is not usable for link performance evaluation in SI simulators due to residual ISI
- MLSE output consists of a sequence of data symbols as opposed to equalized samples
- For IBIS-AMI compliance, construct output waveform from the MLSE output symbols
- This output carries neither timing nor amplitude information for link performance estimation
- MLSE output eye carries symbol error information, while the RX model can provide estimated SNR

Outline

- Motivation
- ADC-Based IBIS-AMI Modeling Challenges
- ADC-Based IBIS-AMI Modeling Methodologies
  - COM-Representative ADC-Based Models
  - Architecturally-Representative ADC-Based Models
  - Maximum Likelihood Sequence Estimation (MLSE) Models
- **SNR-Centric Model Correlation Methodology**
- Conclusion

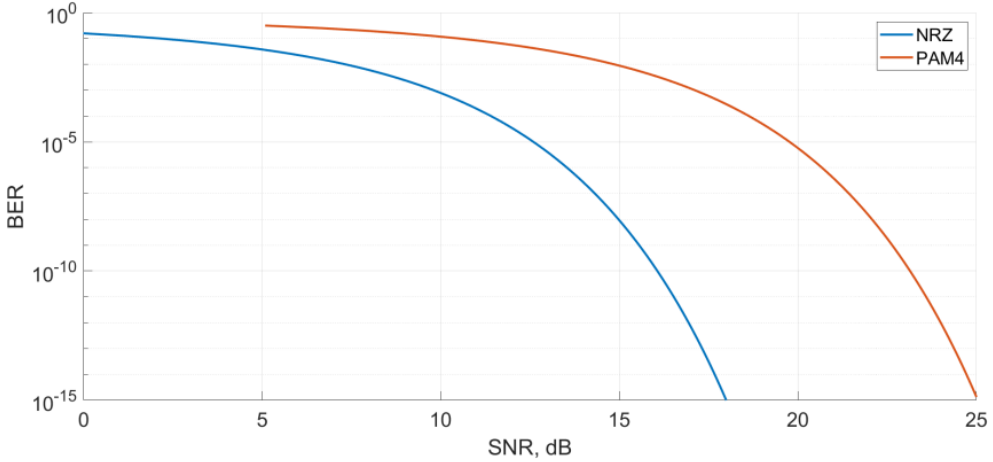
Link Correlation: SNR/BER

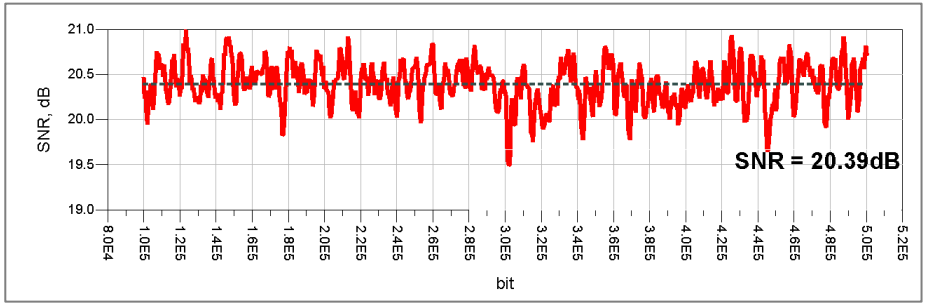
- Measurable:
  - Raw BER is measurable in lab using BIST by counting errors between sent and received symbols

$$BER = \left(\frac{3}{8}\right) erfc\left(\sqrt{\frac{10^{\frac{SNR}{10}}}{10}}\right)$$

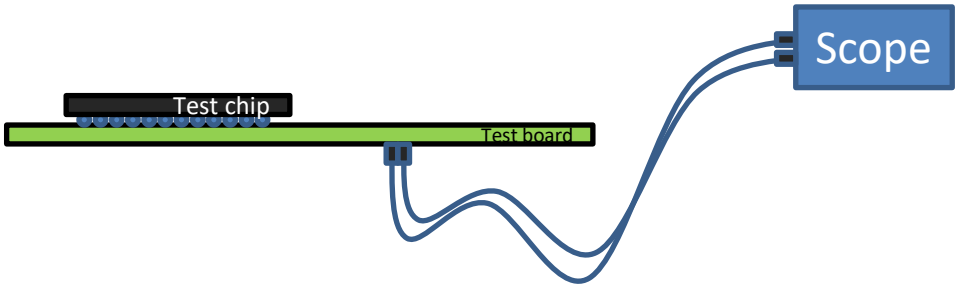
PAM4 signaling BER/SNR relationship

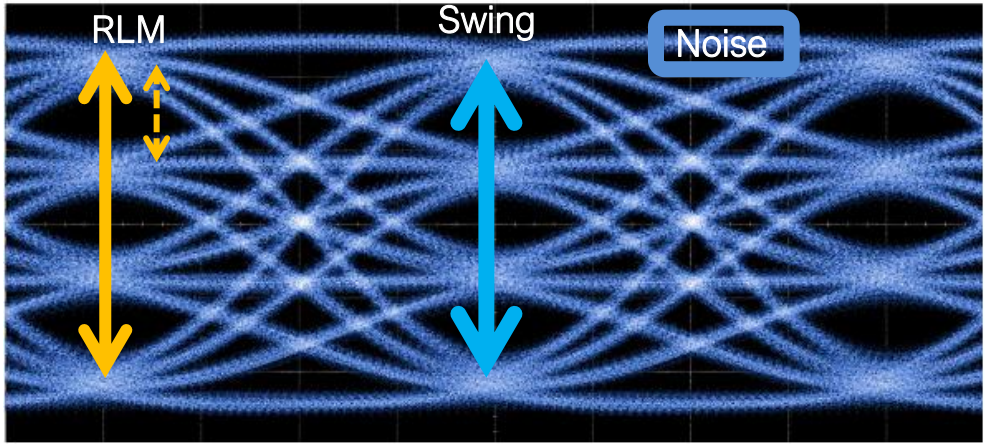
- SNR can be simulated/calculated from IBIS-AMI simulation
  - BER indirectly mapped from SNR using relationship



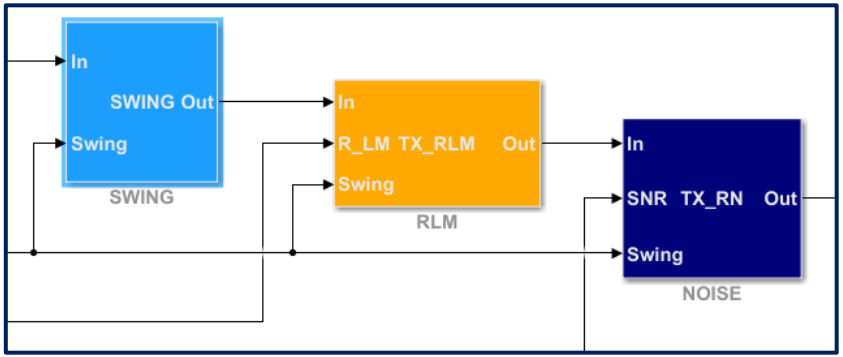


TX Correlation





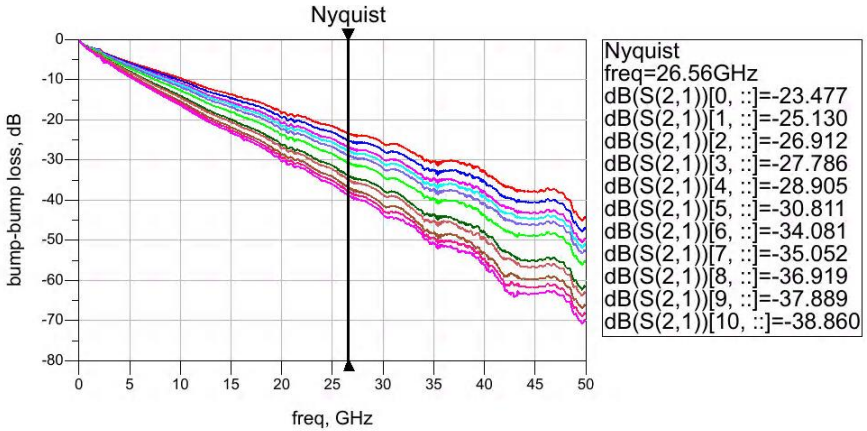
TX IBIS-AMI model block diagram

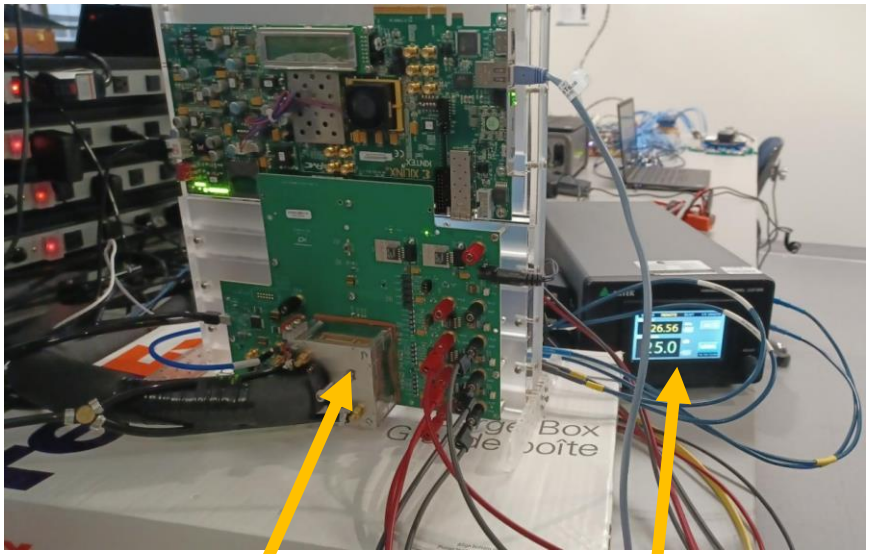


Transmitter is characterized through measurements where behavioural parameters of the transmitter model are extracted from the waveform capture

Link Correlation: Setup

Vary bump-bump interconnect loss



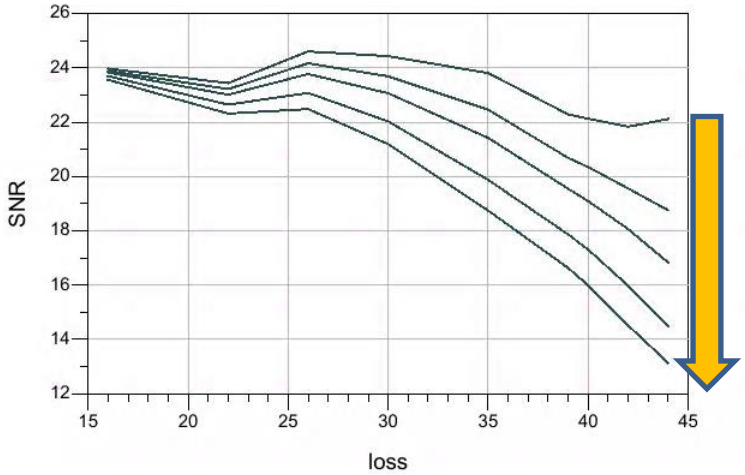


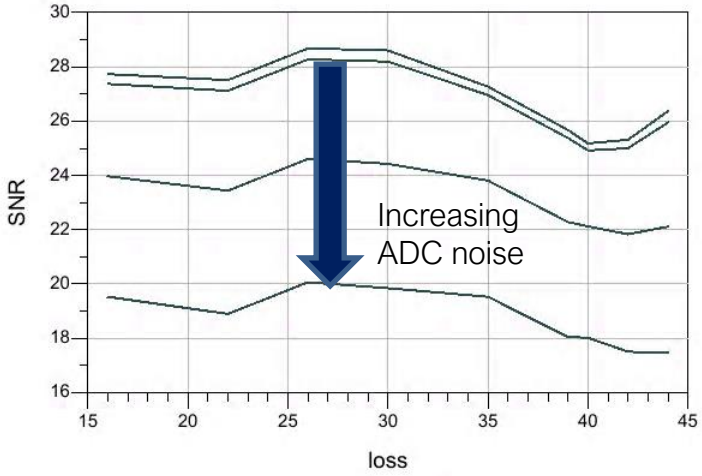
Test chip package with thermal control

Variable ISI channel synthetizer

Link Simulation with RX Noise Sweeps

RX IBIS-AMI model block diagram

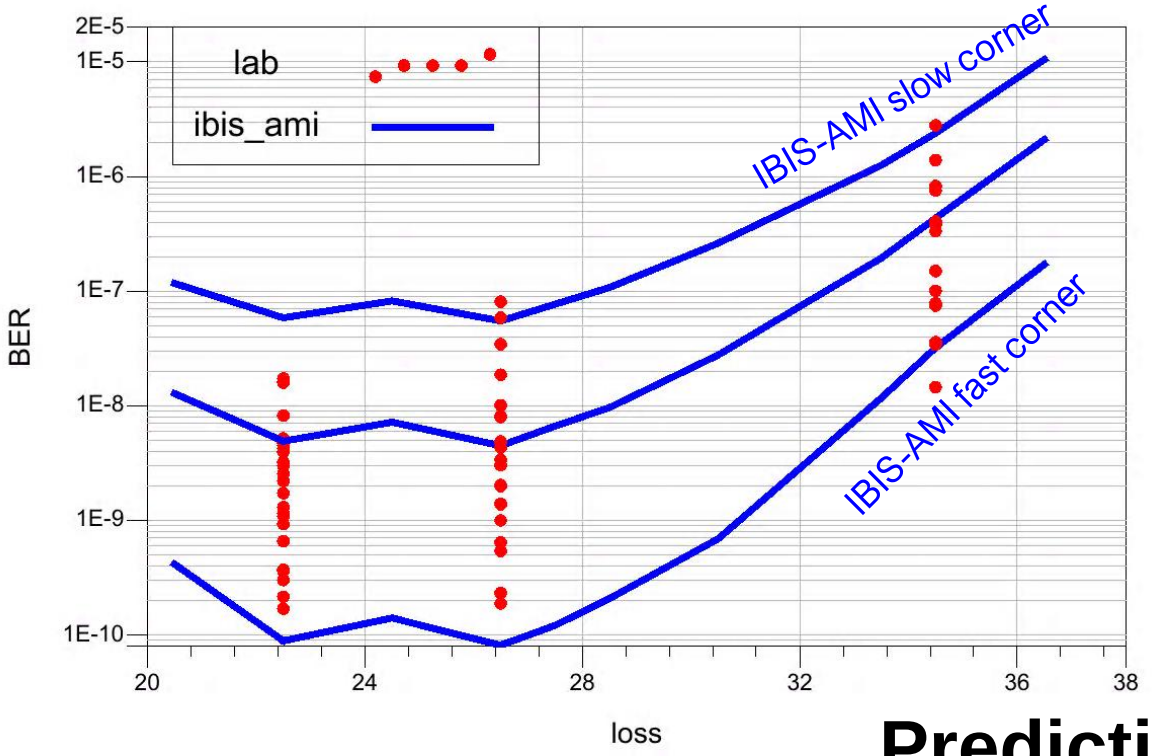




CTLE input referred noise is amplified by the analog-front end chain and have more impacts on longer reach channel

ADC rms noise degrades the link BER/SNR consistently across channel reach

Final Model to Lab Correlation



RX model noise impairment is calibrated to match the performance of the test chip across the loss range

Predictive IBIS-AMI model

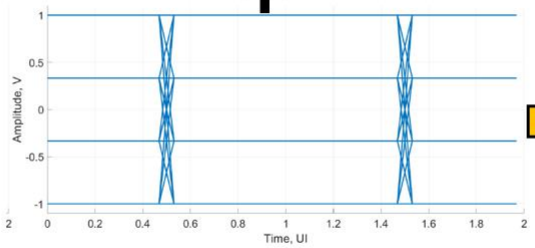
MLSE IBIS-AMI Model

The MLSE Viterbi algorithm is implemented inside the AMI model,

MLSE
AMI RX

Sampling phase

+



Raw BER

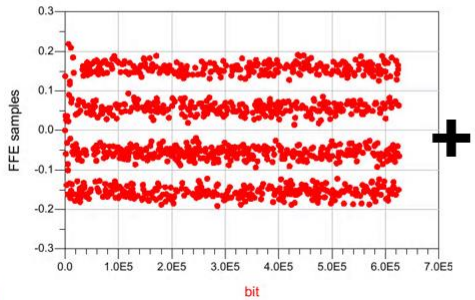
MLSE recovered sequence

3 2 1 3 2 2 0 **1** 0 2 0 1 3 2

input symbol sequence

3 2 1 3 2 2 0 0 0 2 0 1 3 2

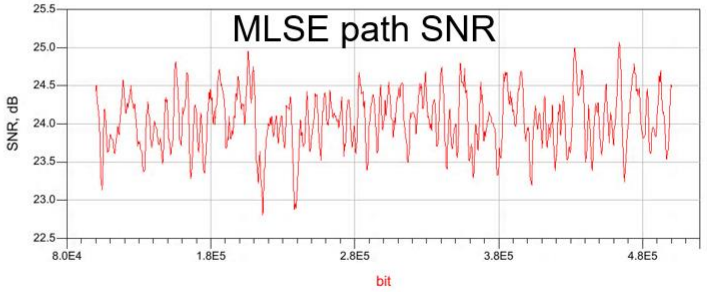
Using MLSE symbol decisions and the prior stage FFE samples voltage constellation we can derive an estimated SNR performance of the MLSE path



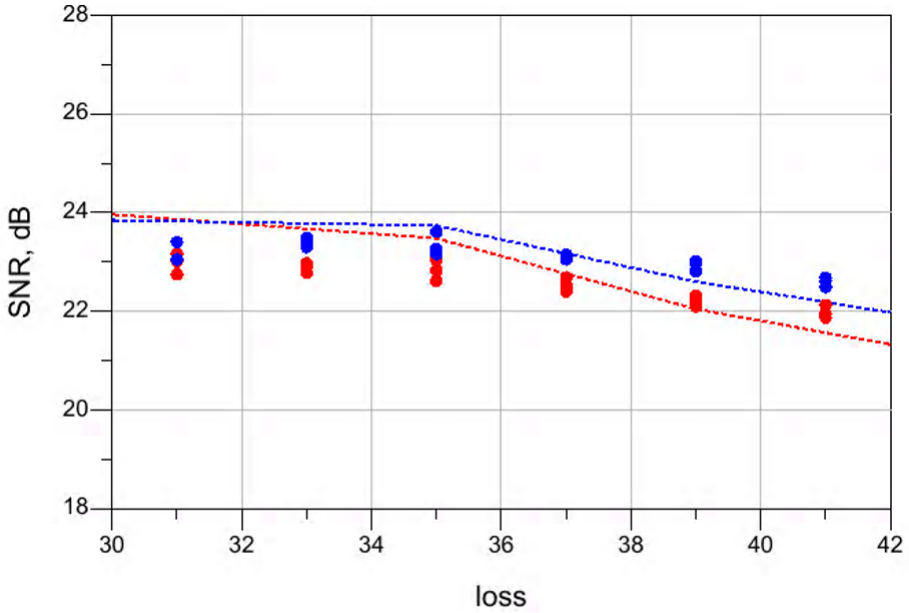
+ MLSE recovered sequence

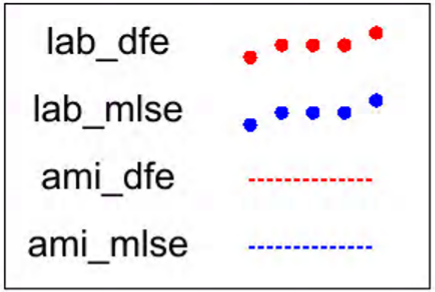
3 2 1 3 2 2 0 1 0 2 0 1 3 2

=



MLSE IBIS-AMI Simulation





0.5dB SNR gain by MLSE for higher reach links can be captured with an AMI simulation of 500k bits simulation

With SNR based approach, we can capture the MLSE performance gain over DFE and predict BER in the order of 1e-8~1e-9 while maintaining a reasonable amount of simulation symbols

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- SNR-Centric Model Correlation Methodology
- **Conclusion**

Conclusion

- Explored challenges of IBIS-AMI modeling for ADC-based SerDes architectures
- Proposed three IBIS-AMI modeling methodologies for ADC-based SerDes
  - COM-Representative ADC-Based Models
  - Architecturally-Representative ADC-Based Models
  - Maximum Likelihood Sequence Estimation (MLSE) Models
- Explored implication of these methodologies on model-simulator interface
- Proposed SNR-based IBIS-AMI correlation methodology
- Used proposed methodologies to build and correlate models for 1-112 Gb/s multi-standard SerDes
- Two RX noise sources were used to drive model correlation
  - Loss-dependent noise at CTLE input
  - Loss-independent noise at ADC input
- Resulting predictive IBIS-AMI models cover SerDes IP performance across measured PVT variation

MORE INFORMATION

- www.serialinksystems.com
- info@serialinksystems.com
- Supporting material
  - https://www.mathworks.com/help/serdes/ug/adc-ibis-ami-model-based-on-com.html
  - https://www.mathworks.com/help/serdes/ug/architectural-112g-pam4-adc-based-serdes-model.html