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Parametric System Model of a 112Gbps ADC-based SerDes for Architectural, Design & Validation Project Phases

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SPEAKER

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SeriaLink Systems is working on building a configurable modeling flow to support SerDes projects through their entire life cycle: from architecture definition, through analog and digital design, to design validation. Aleksey has been working on behavioral modeling of high-speed SerDes systems, architecture analysis, adaptation, and signal integrity with multi-standard SerDes IP teams at V Semi and Intel.

Outline

- Motivation
- System Modeling through SerDes Development
- Parametric DAC-based TX Model
- Parametric ADC-based RX Model
- Model Correlation
- Conclusion

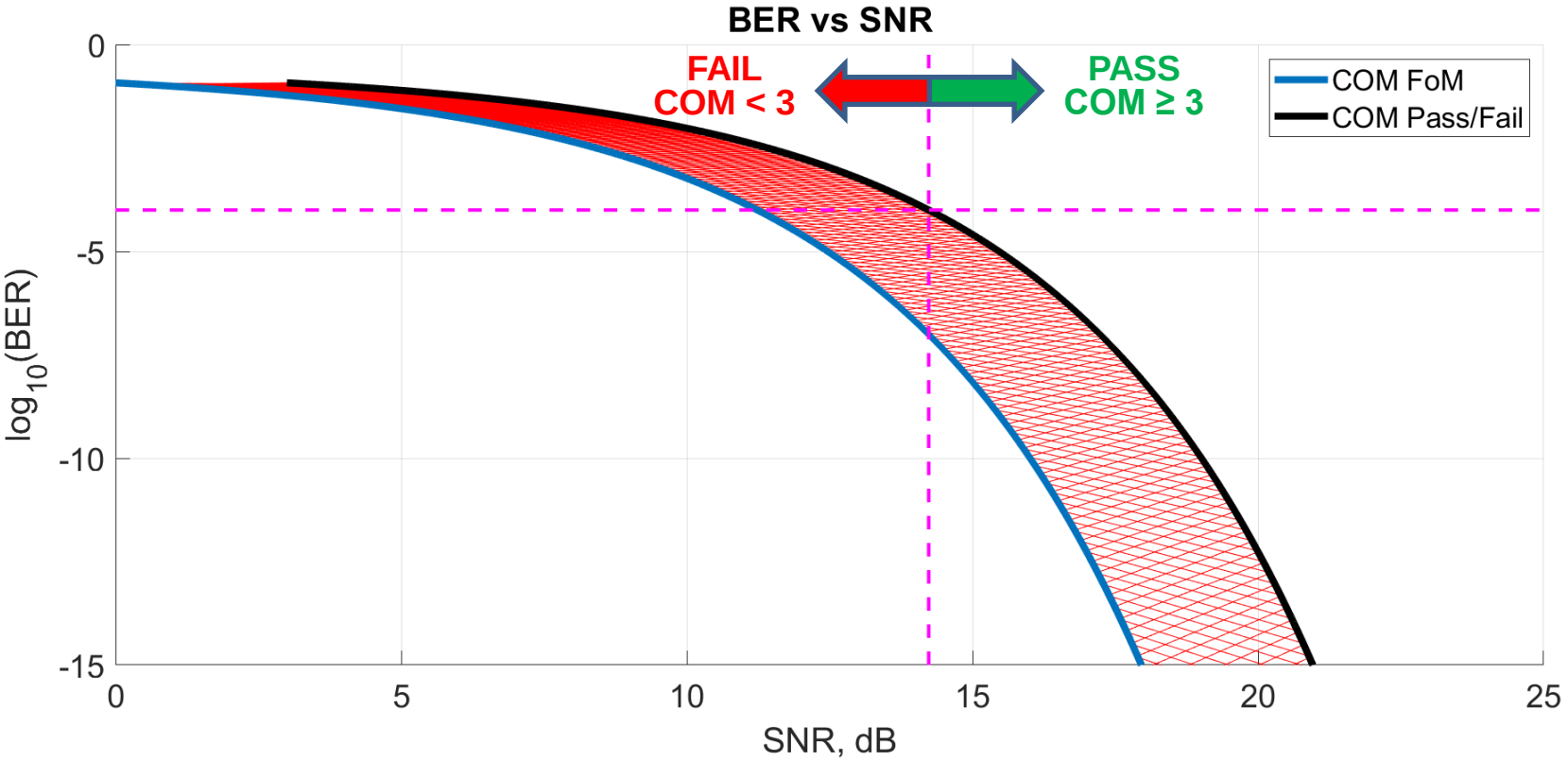
Motivation

- Multiple system models support SerDes IP development
- These internal development models are rarely shared with system integrators
- At leading-edge data rates, SerDes IP and channels are developed concurrently

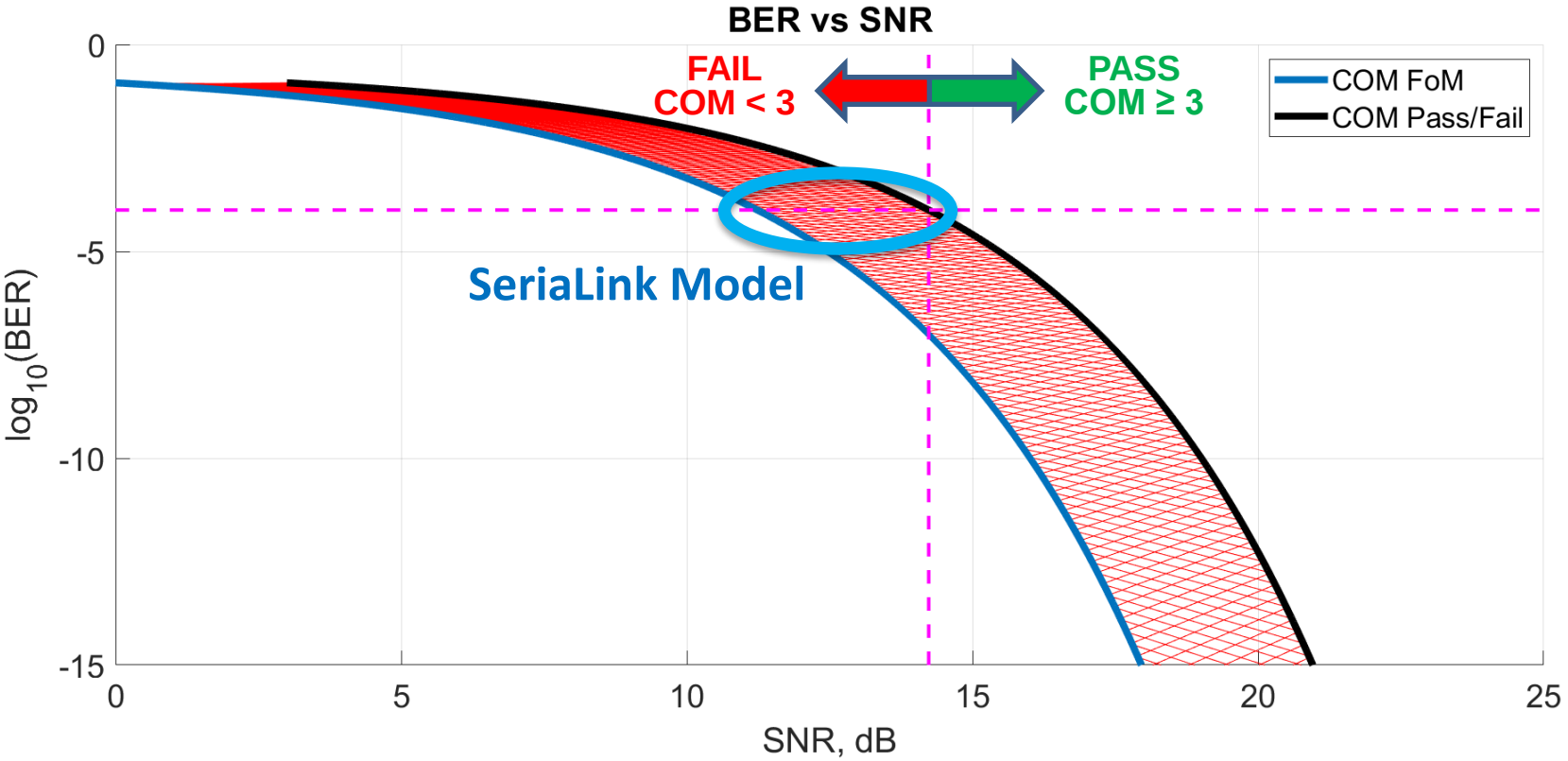
- However, limited modeling options available for technical interaction
- COM drives specification alignment at the project onset
- IBIS-AMI drives signal integrity sign-off at the project end
- During majority of design activities, models suitable for sharing are unavailable

- Is it possible to unify SerDes system modeling activities into a single framework?
- Can the unified models facilitate technical interaction between IP vendors and system integrators?

COM Implementation Margin



COM Implementation Margin



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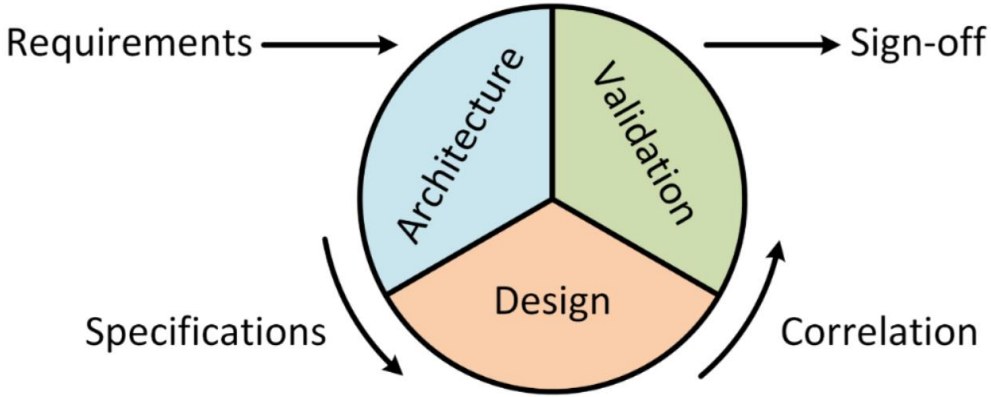
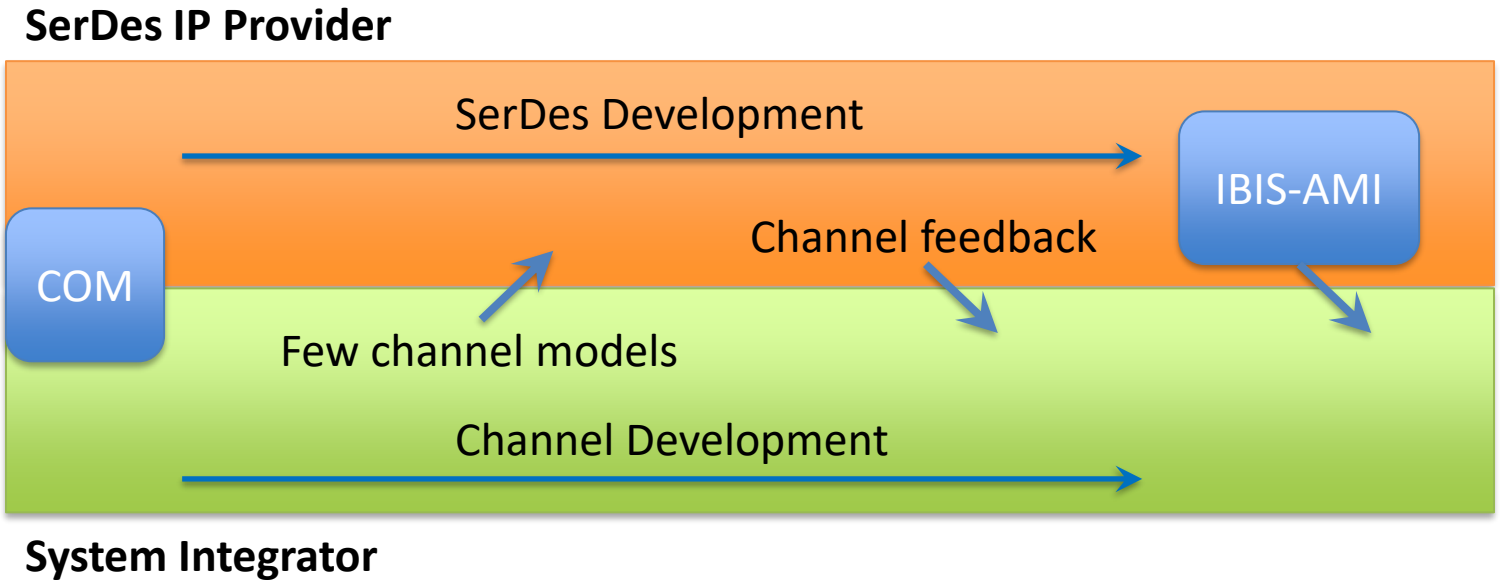
System Models in SerDes IP Development



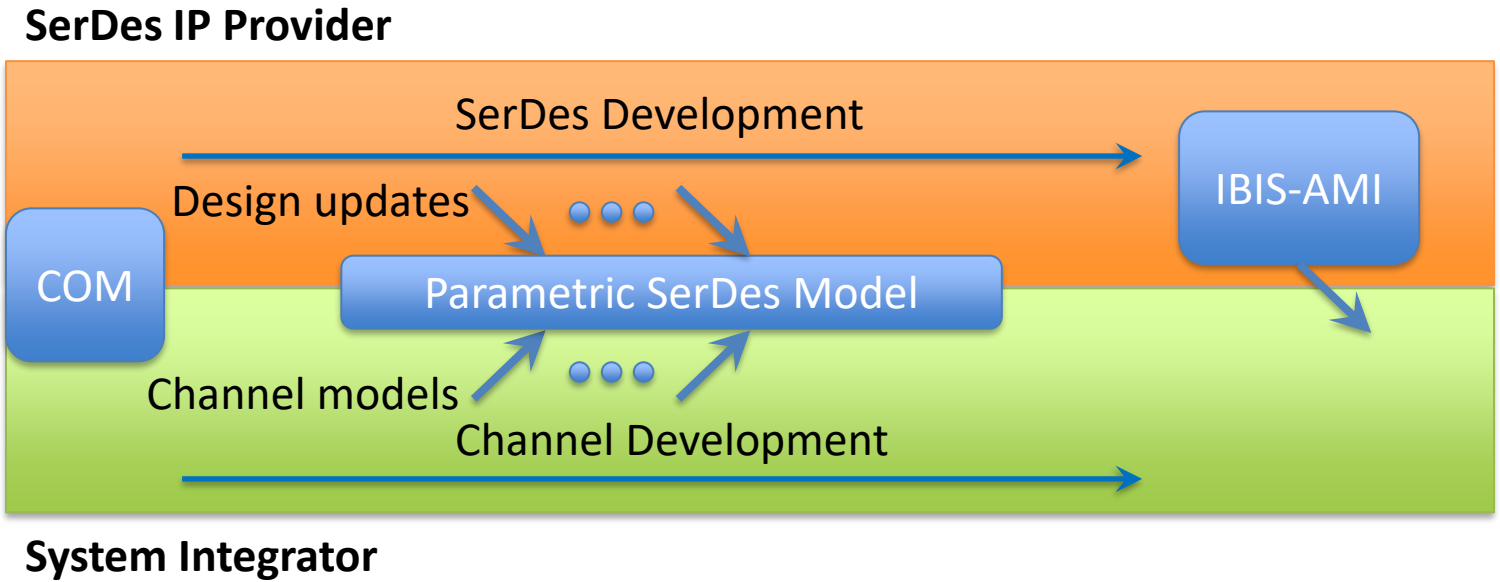
- Multiple system models support SerDes IP development activities
- Approximate (abstract) models guide architectural exploration and design specifications
- Detailed models support design activities by evaluating performance trade-offs between different blocks
- Port-accurate correlated models drive mixed-signal validation before project sign-off
- These individual models are rarely shared with system integrators due to logistics and IP protection concerns
- Proposed unified modeling framework can replace multiple models with one model, suitable for sharing

Interaction: IP Supplies and System Integrators



- COM facilitates alignment at the project onset, for standard-compliant and custom SerDes systems
- IBIS-AMI enables signal integrity validation and sign-off at the end of the development cycle
- No suitable models are available for sharing during the majority of design activities

Interaction: IP Supplies and System Integrators



- Augment COM and IBIS-AMI with a parametric SerDes model that reflects IP performance
- Obfuscated code at block level for IP protection, exposed top level signals for observability
- Quantitative feedback between teams early in development process, in a regressable self-contained test-bench

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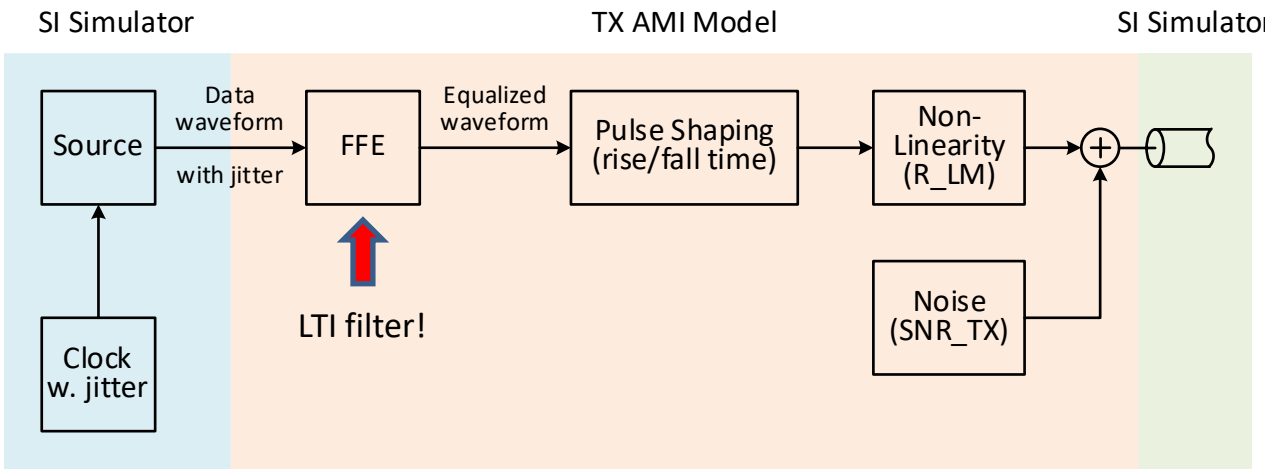
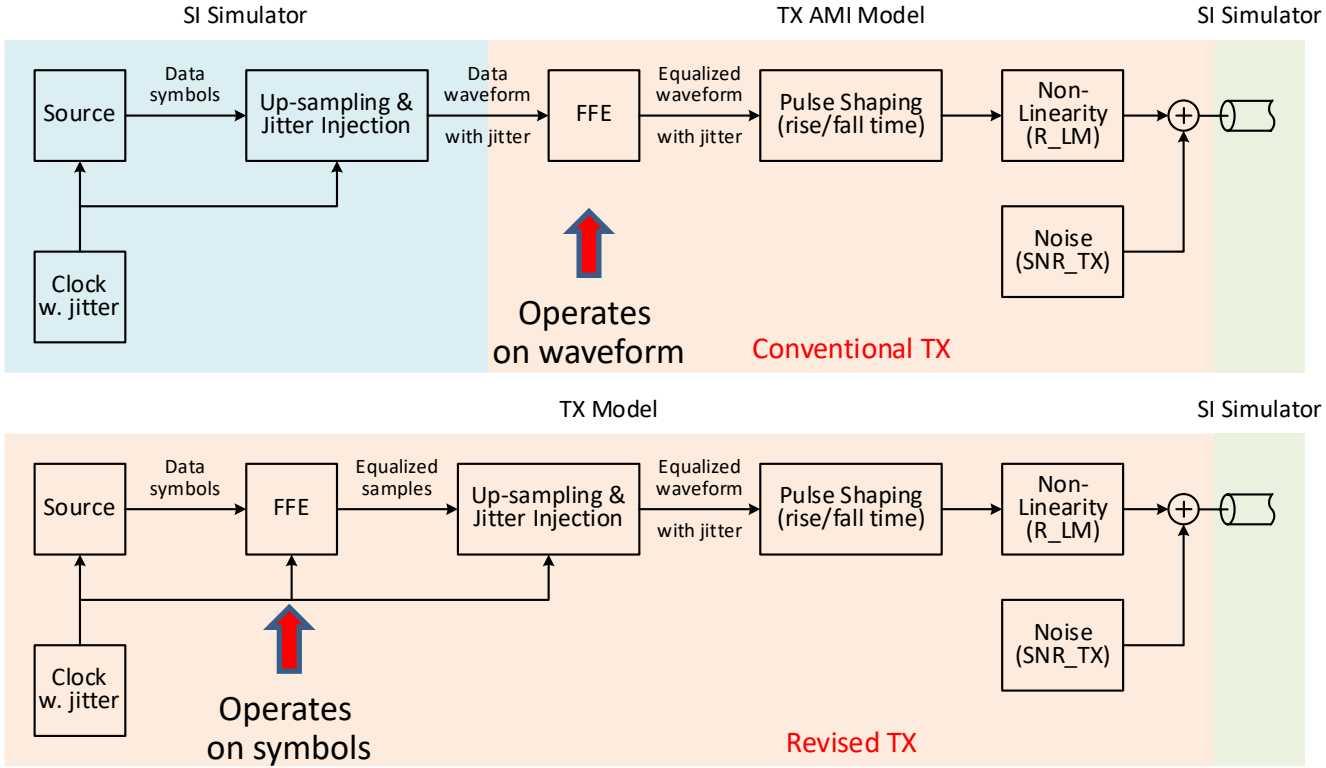
COM-parametric TX Model in IBIS-AMI Framework

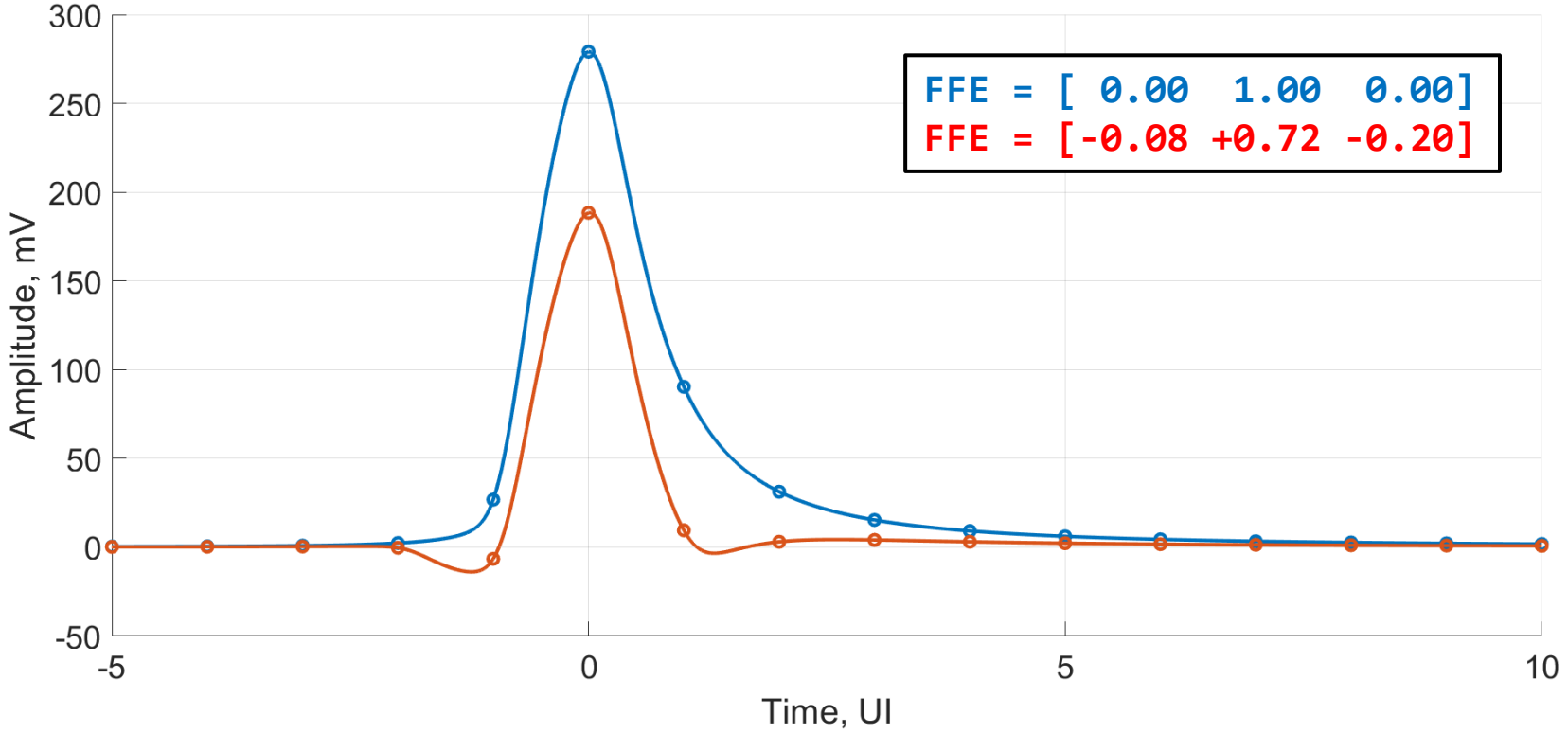


- Includes same components as COM reference TX, supports statistical and time domain simulations
- COM-parametric TX model with two intended use cases
  - Can be configured to represent a standard-compliant TX
  - Can be configured to represent measured TX performance

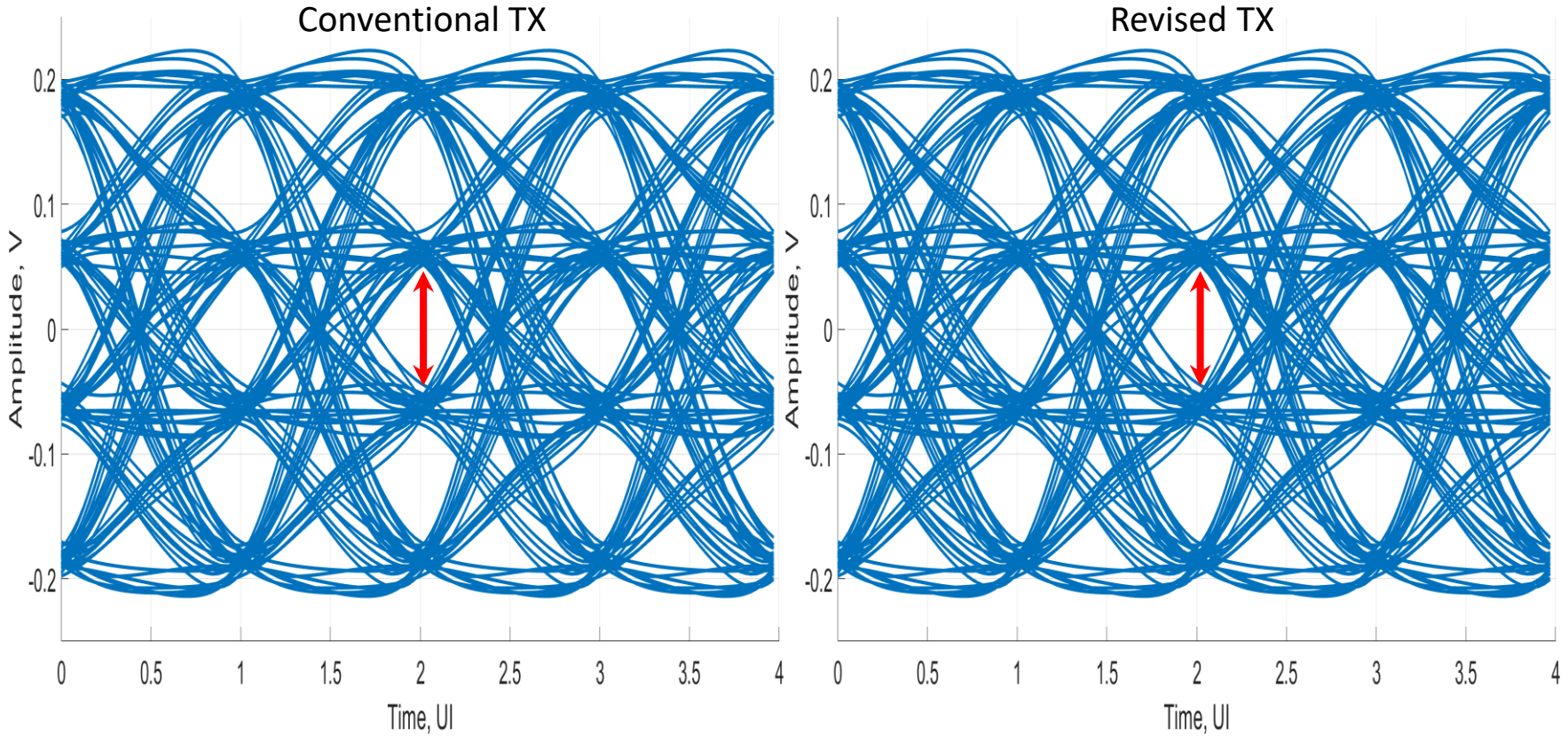
Revised TX Model



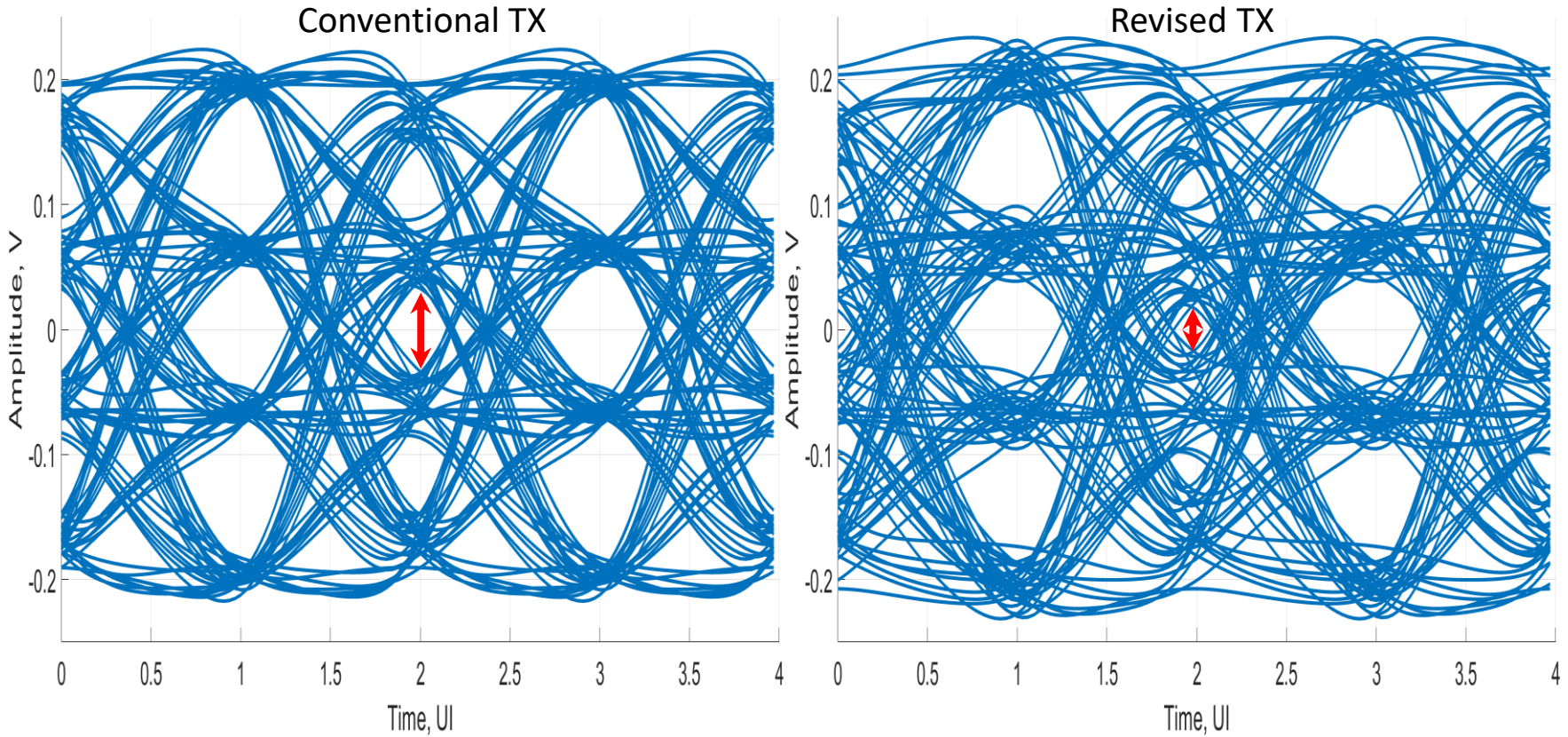
Channel Response: IL = 10 dB



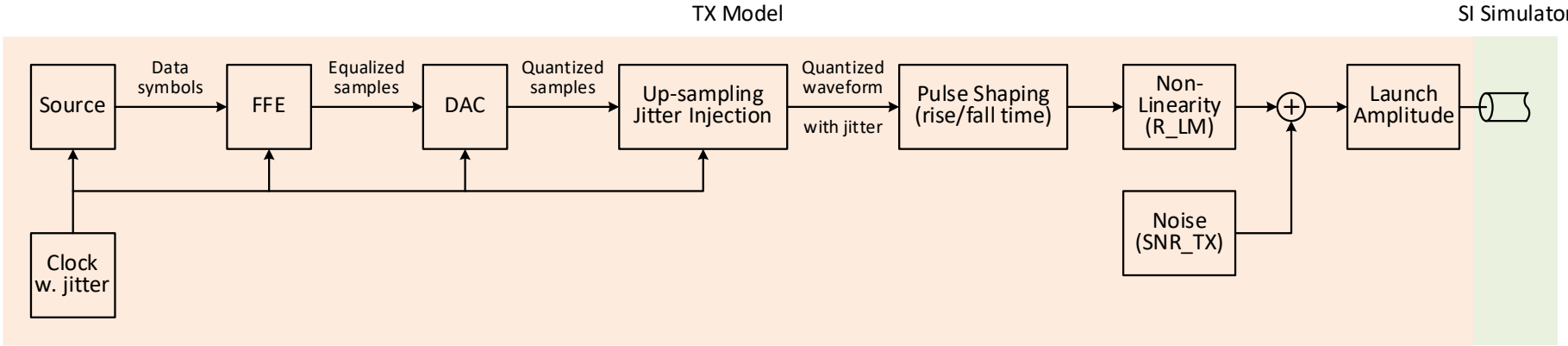
FFE = [-0.08, +0.72, -0.20], IL = 10dB, DCD = 0 mUI_P



FFE = [-0.08, +0.72, -0.20], IL = 10dB, DCD = 75 mUI_P

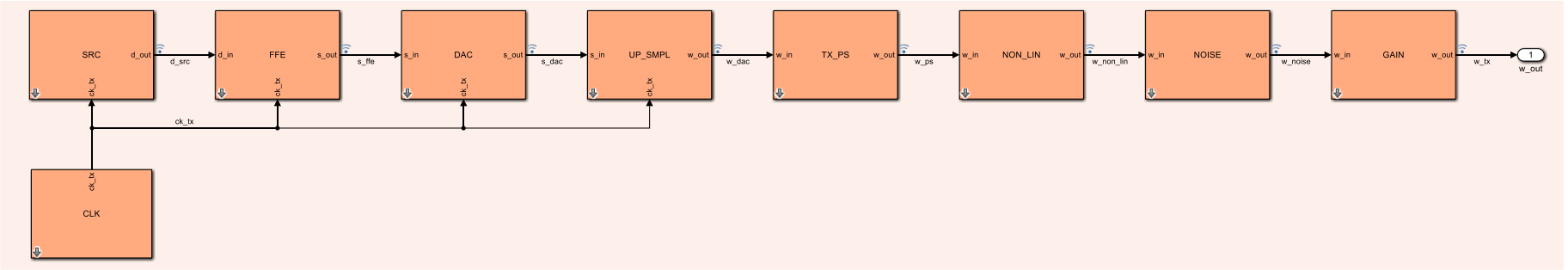


Proposed DAC-based TX Model



- Access to equalized samples enables modeling DAC-based TX architectures
- Direct access to data bits and symbols opens up an option to add FEC into the link model
- Enables exploration of higher order PAM modulations
- Blocks are instances of corresponding classes, configured at simulation start
- Block implementation can be obfuscated for IP protection when models are shared with system integrators
- All signals between blocks remain observable

Proposed DAC-based TX Model in Simulink



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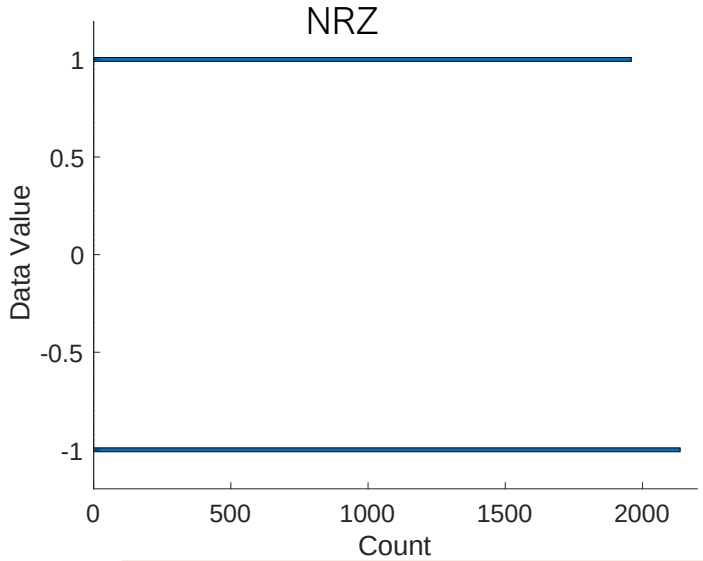
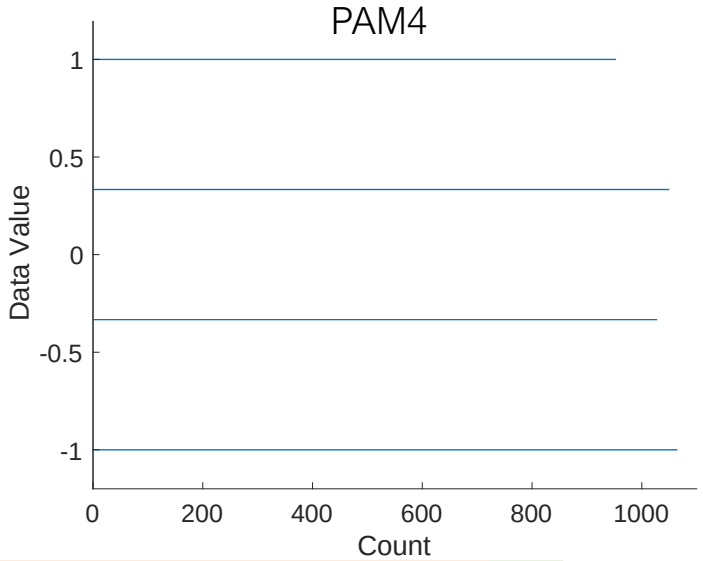
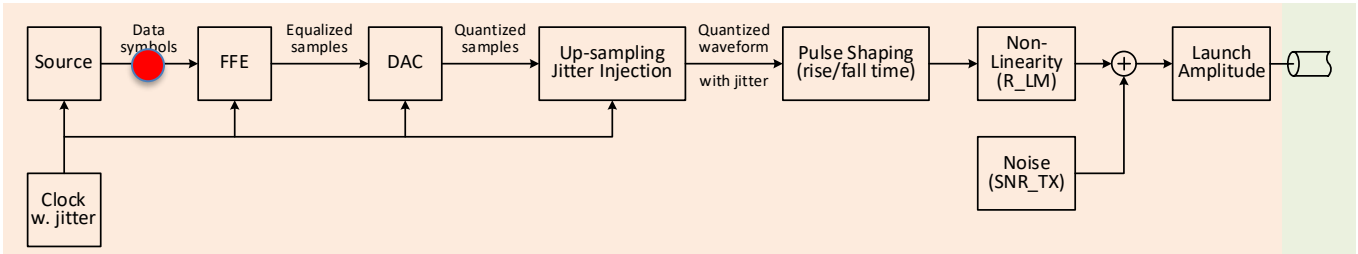
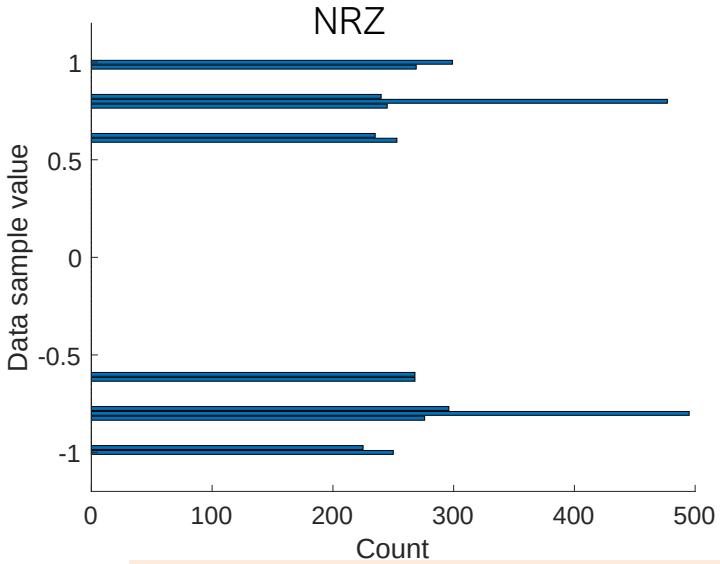
TX Model Observability: Data Source

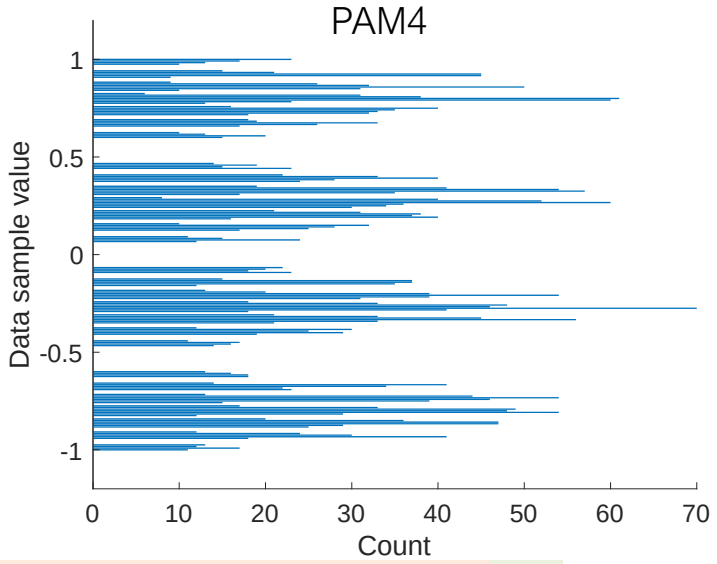


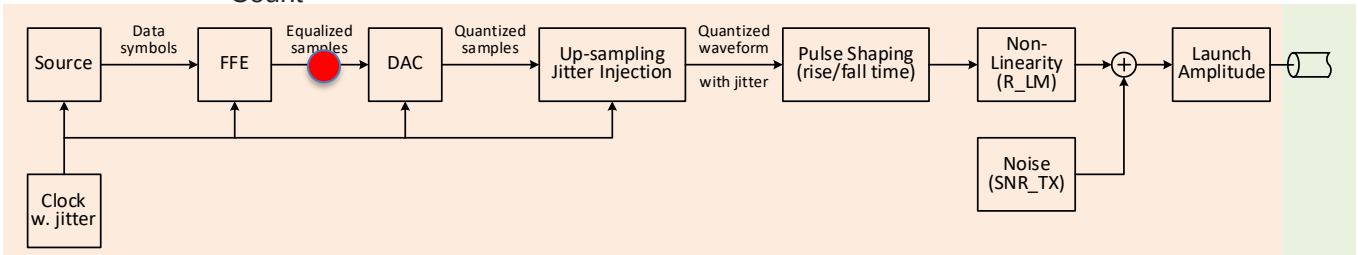




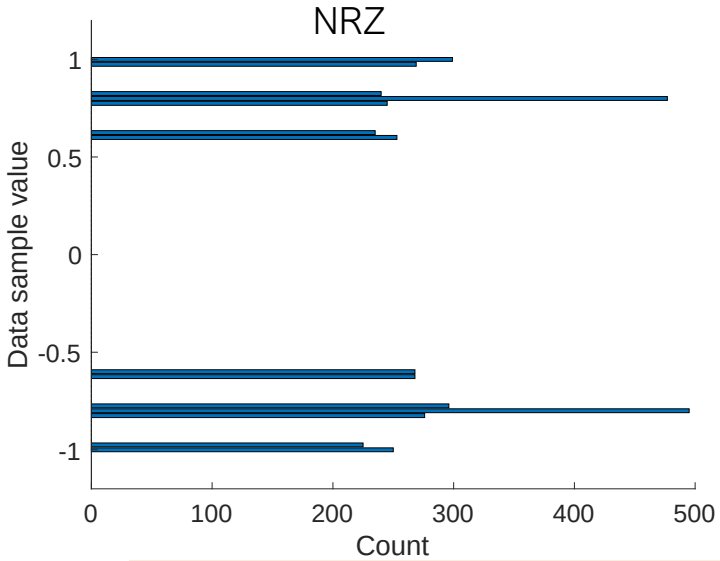
TX Model Observability: FFE

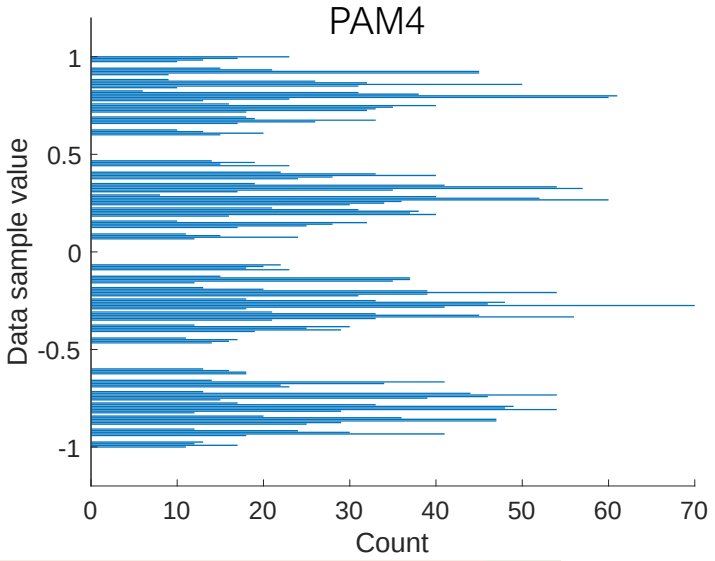


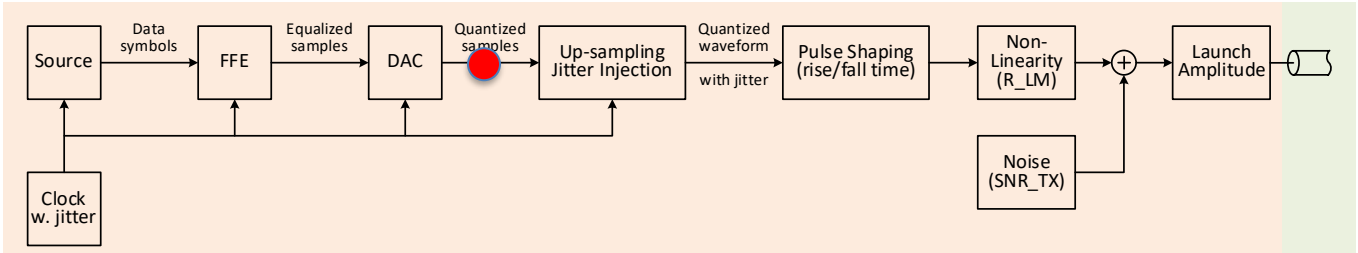




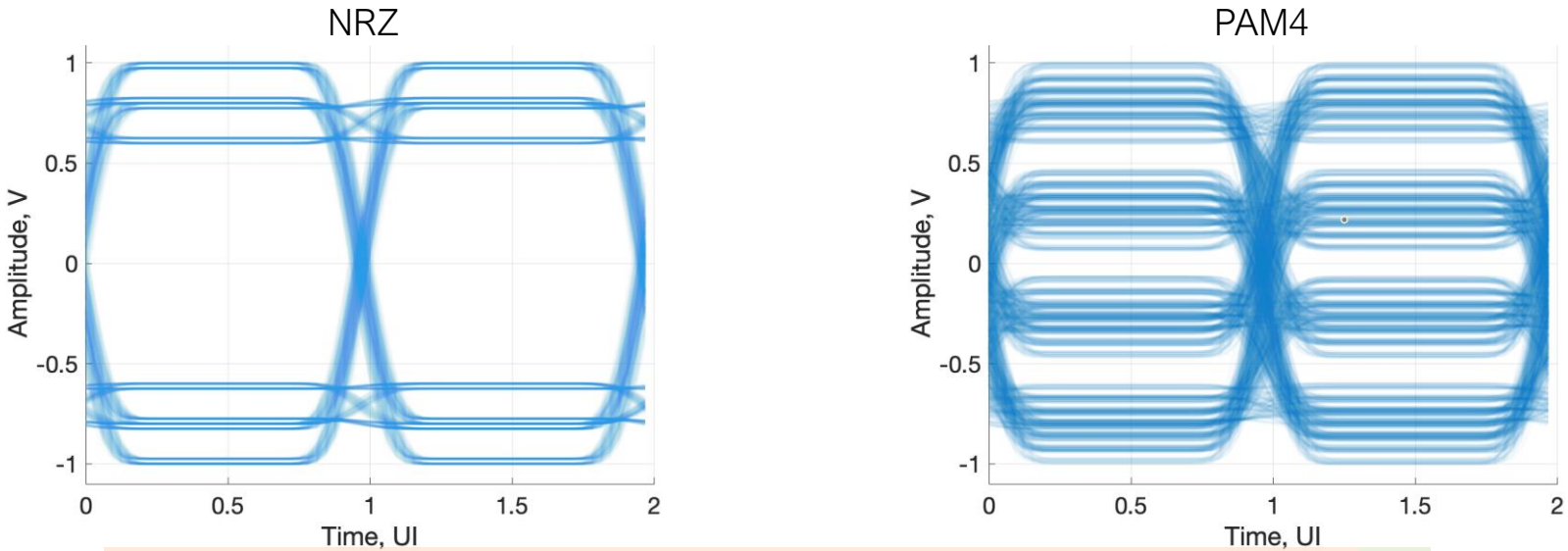
TX Model Observability: DAC



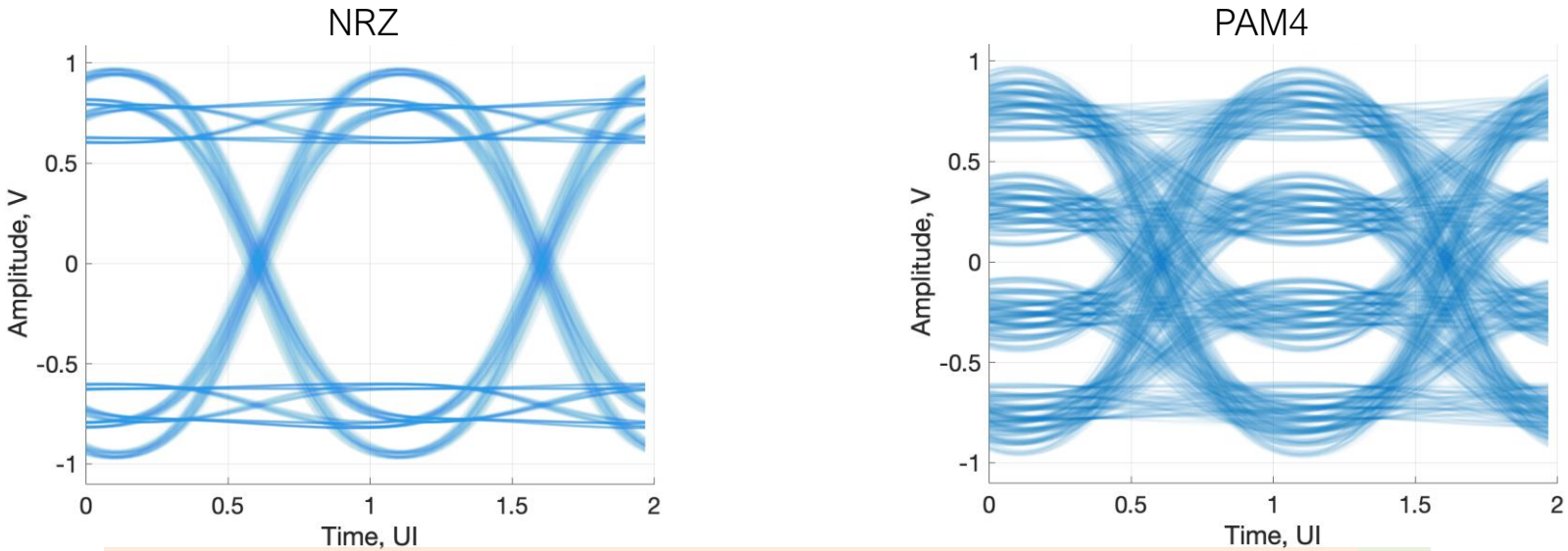




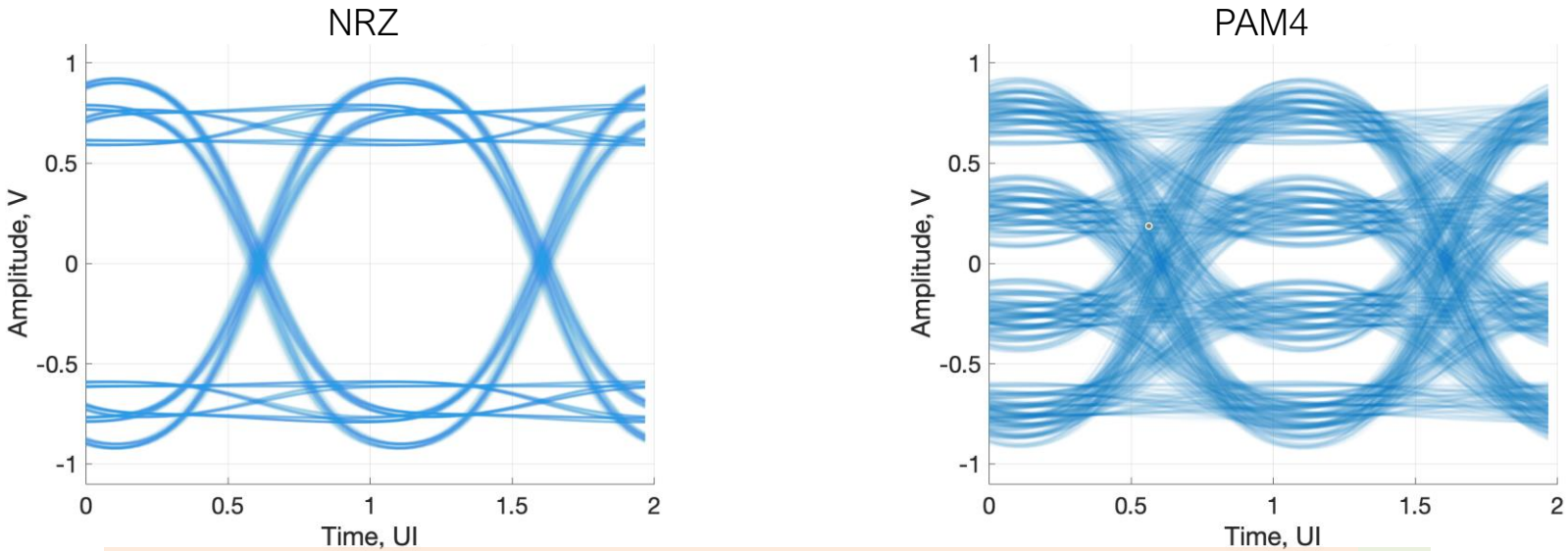
TX Model Observability: Jitter Injection

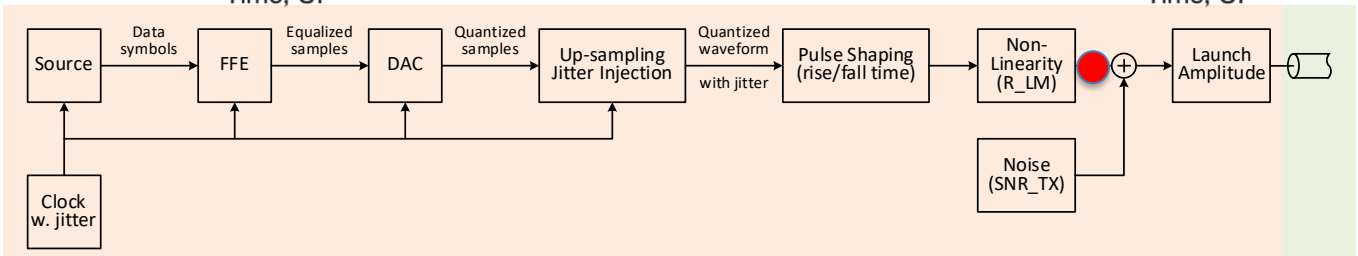


TX Model Observability: Rise/Fall Time Adjust

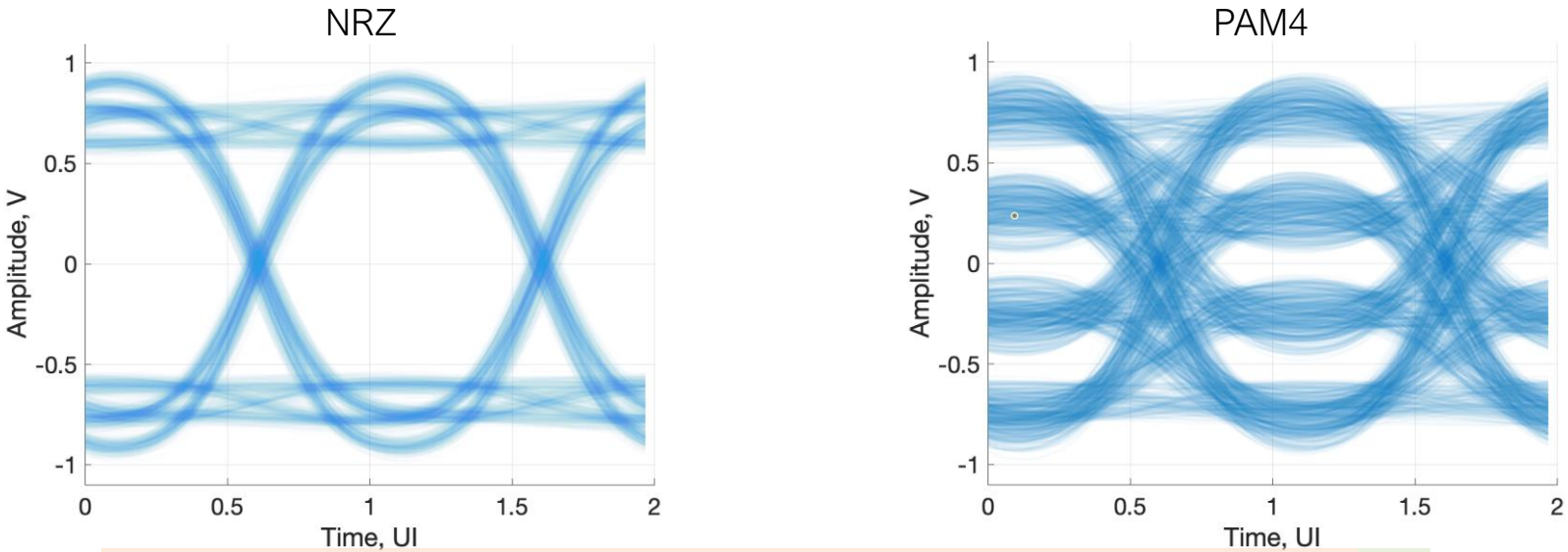


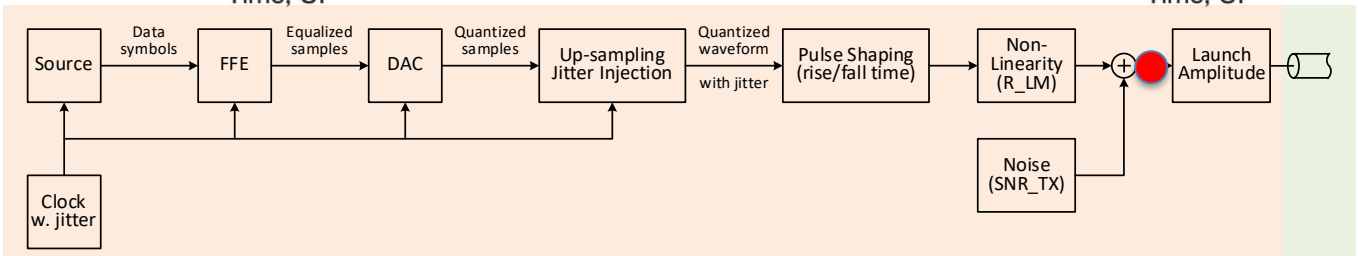
TX Model Observability: Non-Linearity



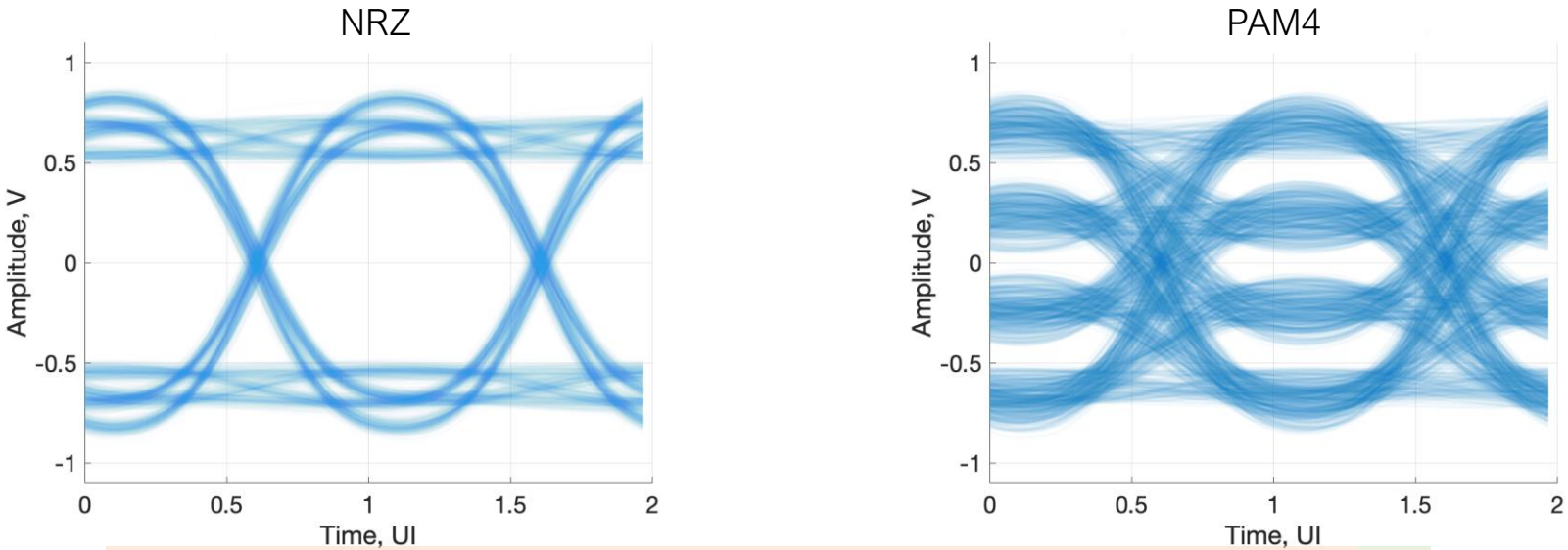


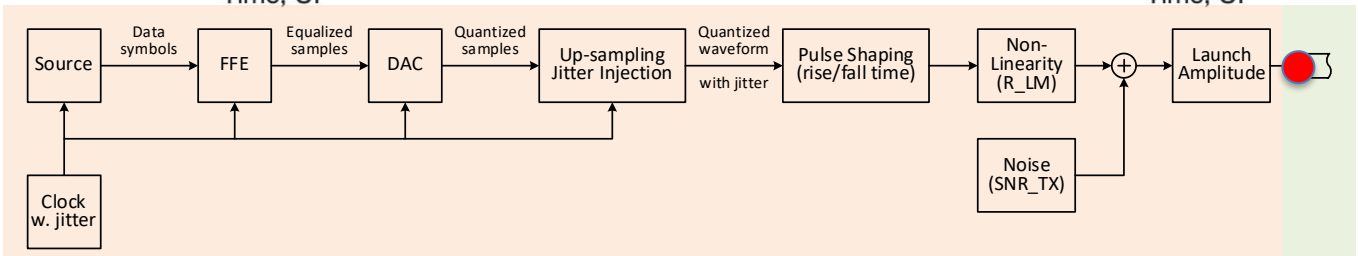
TX Model Observability: Noise





TX Model Observability: Launch Amplitude





TX Model Configurability

	COM	SeriaLink Model
Data pattern: PRBS sequence, repeating pattern, data from file	✗	✓
Modulation	✓	✓
Number of FFE taps, tap ranges	✓	✓
DAC resolution	✗	✓
Basic jitter sources	✓	✓
Advanced jitter sources	✗	✓
Rise / fall time, launch amplitude	✓	✓
Non-linearity, voltage noise	✓	✓
Time domain simulations	✗	✓

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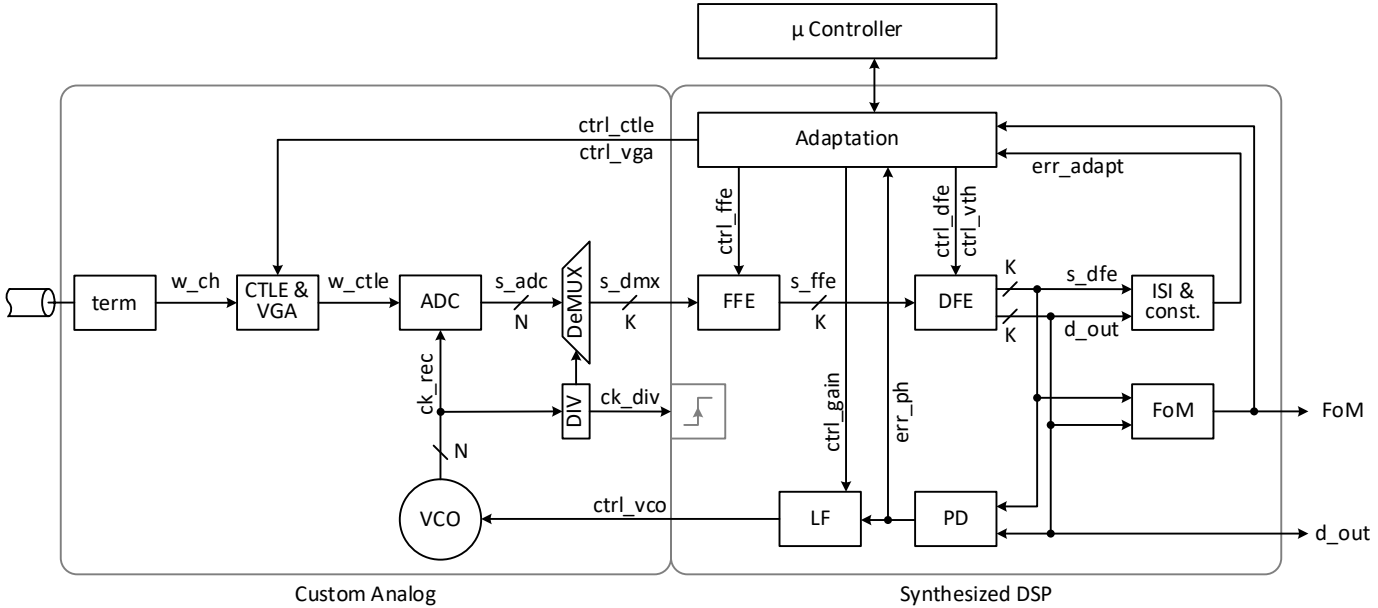
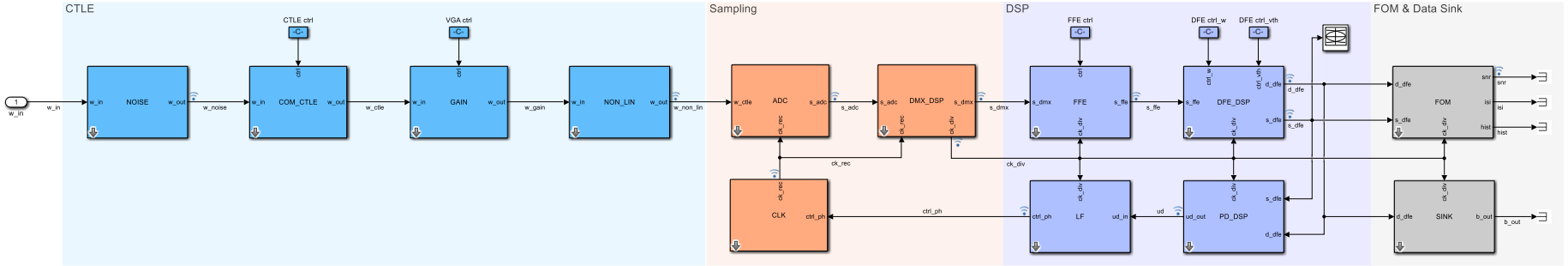
Proposed ADC-based RX Model



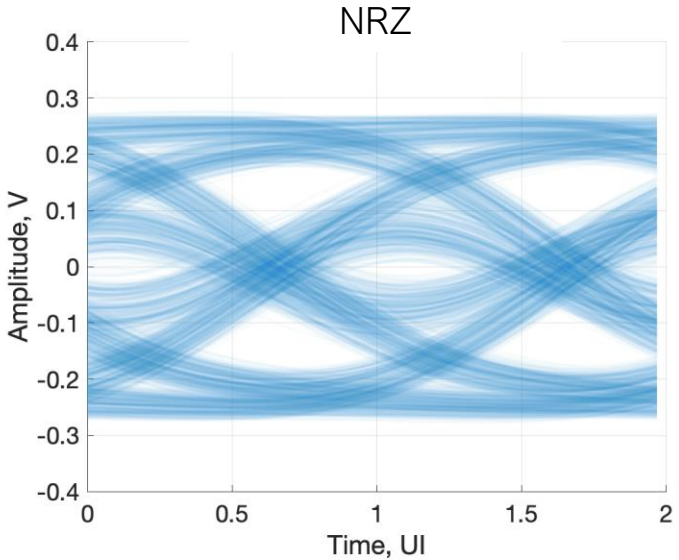
- Design-representative RX model, includes top-level blocks with their interfaces
- Configurable CTLE, time-interleaved ADC sampling, frame-based DSP
- Representative block interfaces allow modeling calibration and adaptation in time domain

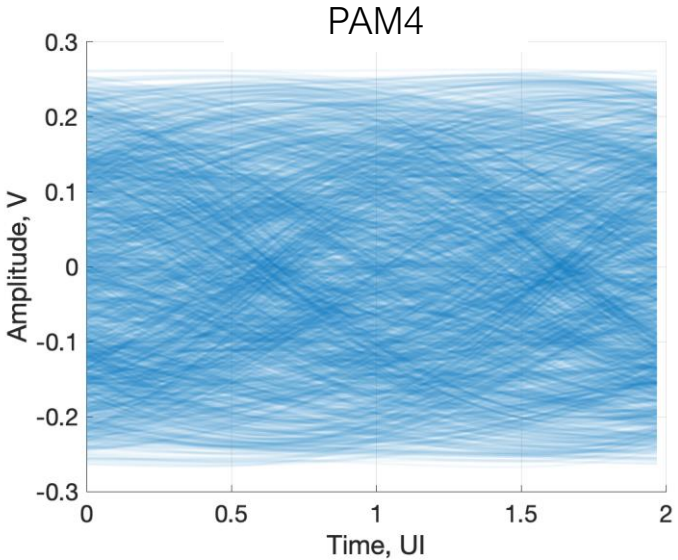
Proposed ADC-based RX Model in Simulink

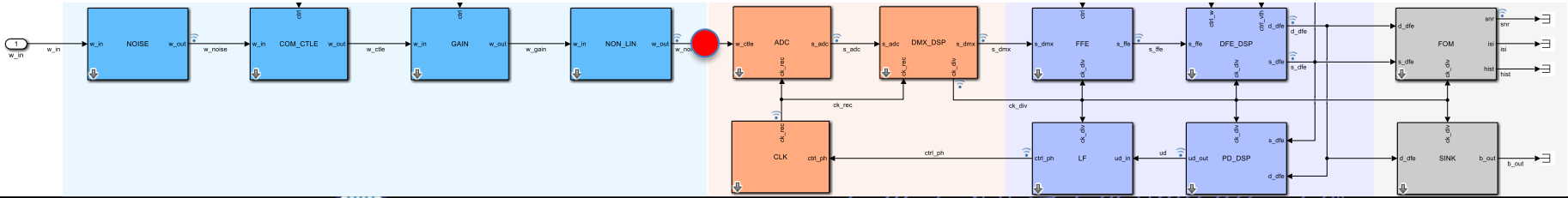


- Blocks can be added or removed to focus on a certain aspect of SerDes behavior
- Direct access to data bits and symbols opens up an option to add FEC into the link model
- Enables exploration of higher order PAM modulations
- Blocks are instances of corresponding classes, configured at simulation start
- Block implementation can be obfuscated for IP protection when models are shared with system integrators
- All signals between blocks remain observable

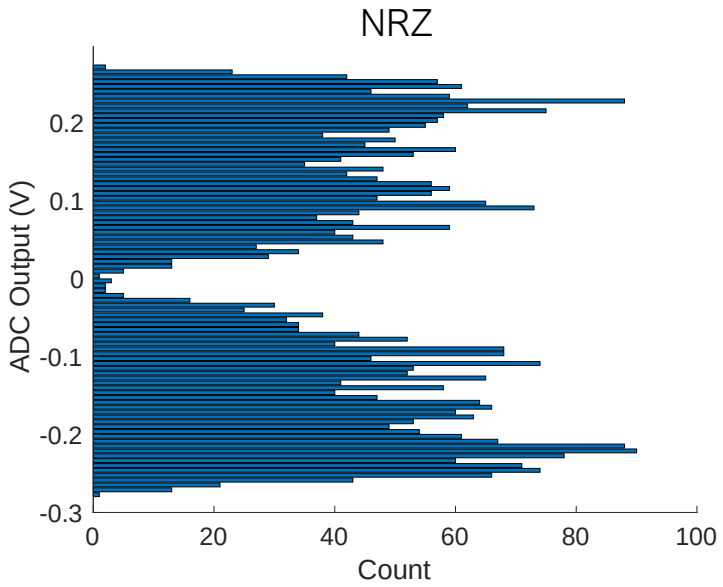
RX Model Observability: CTLE

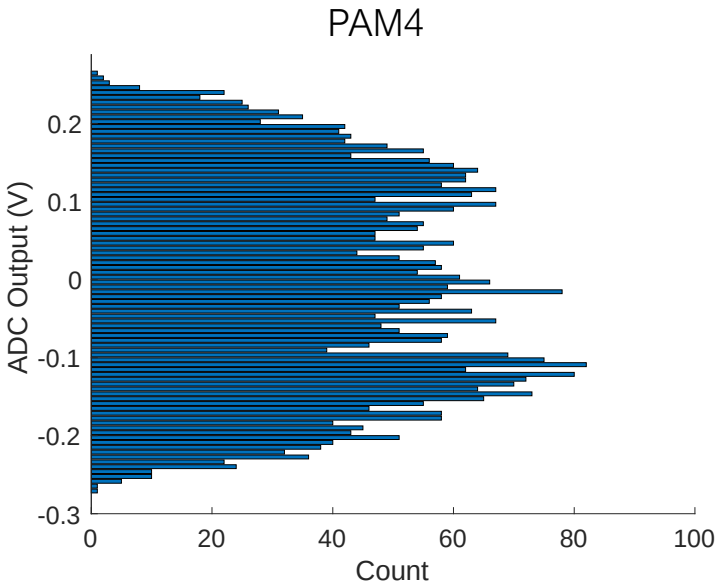


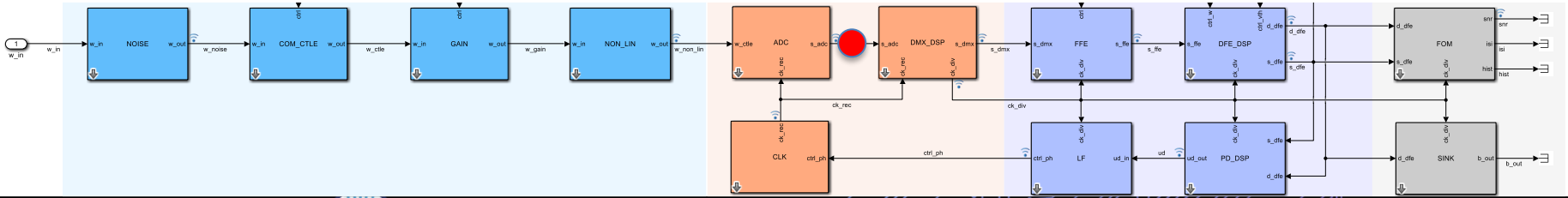




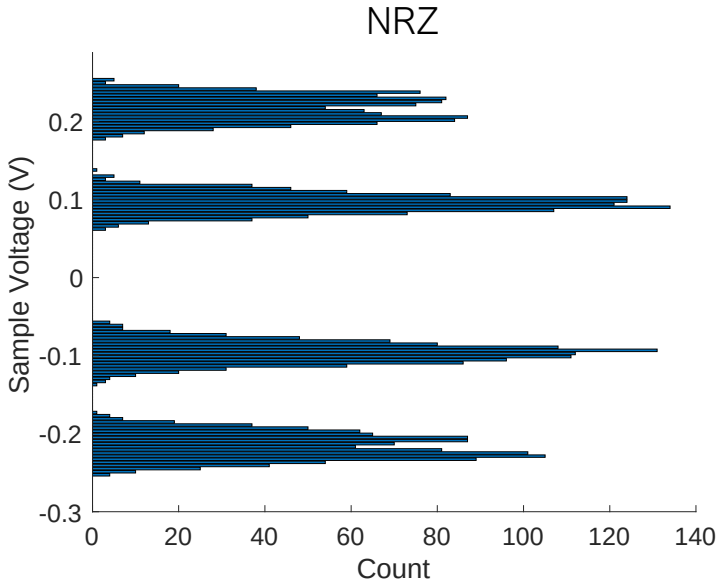
RX Model Observability: ADC

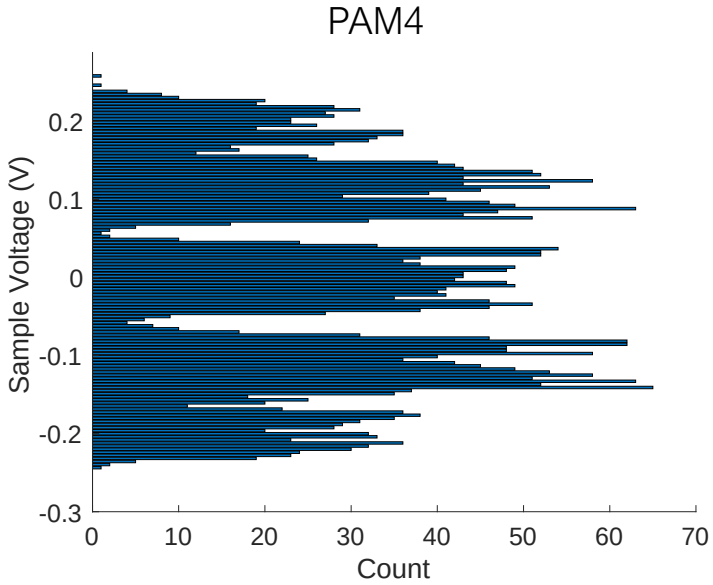


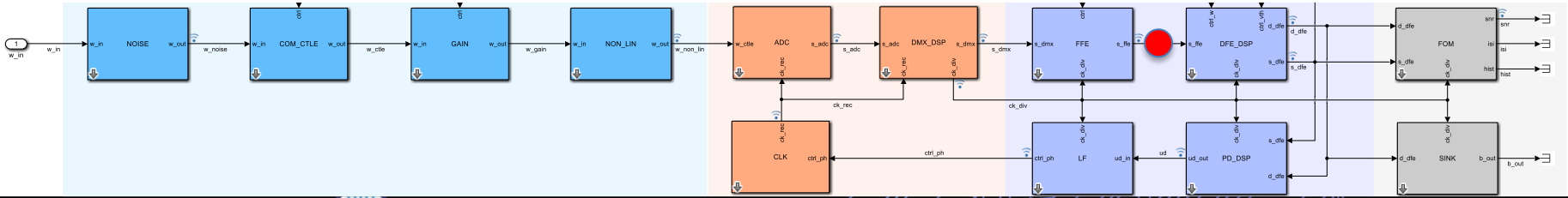




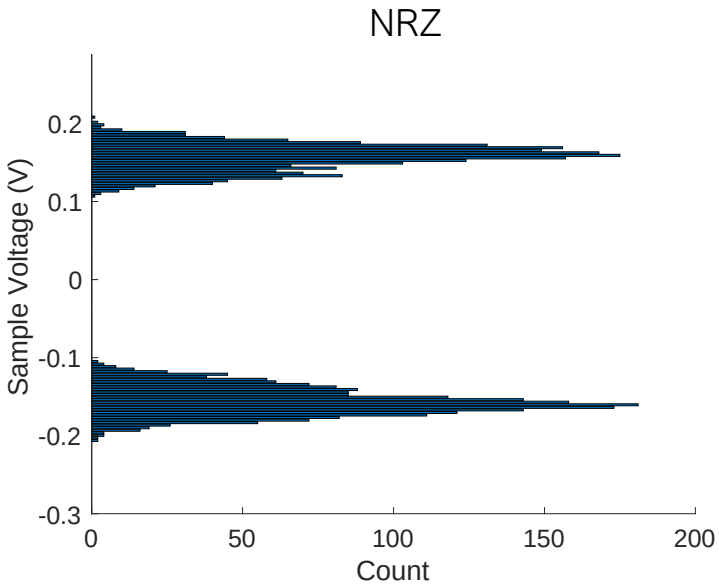
RX Model Observability: FFE

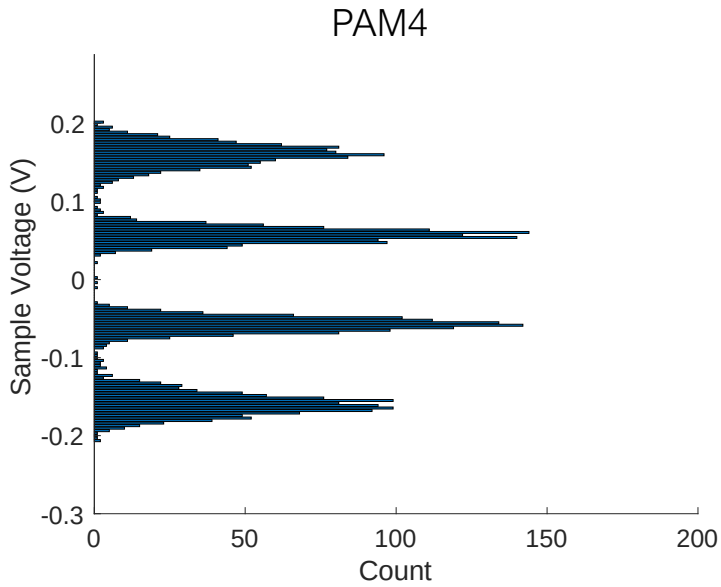


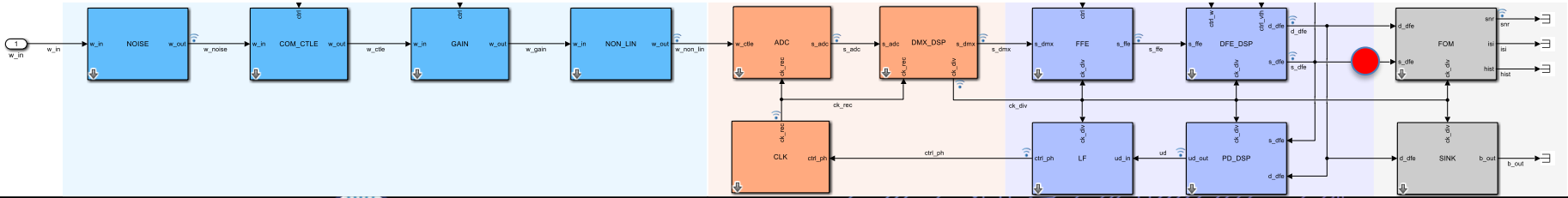




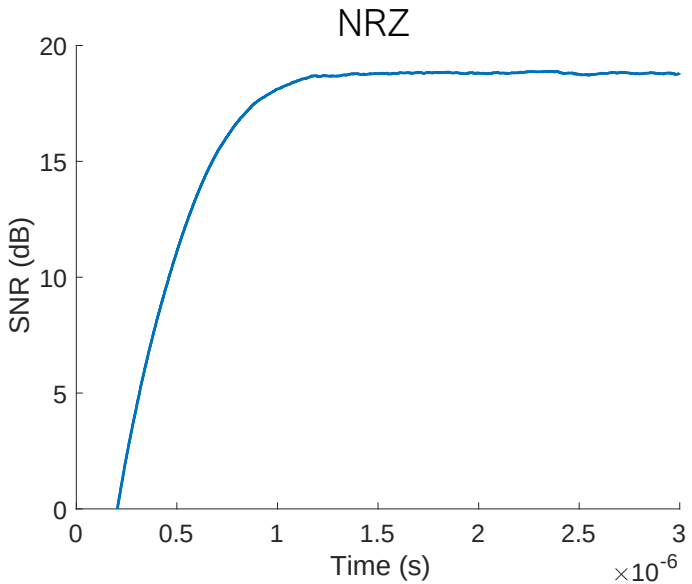
RX Model Observability: DFE

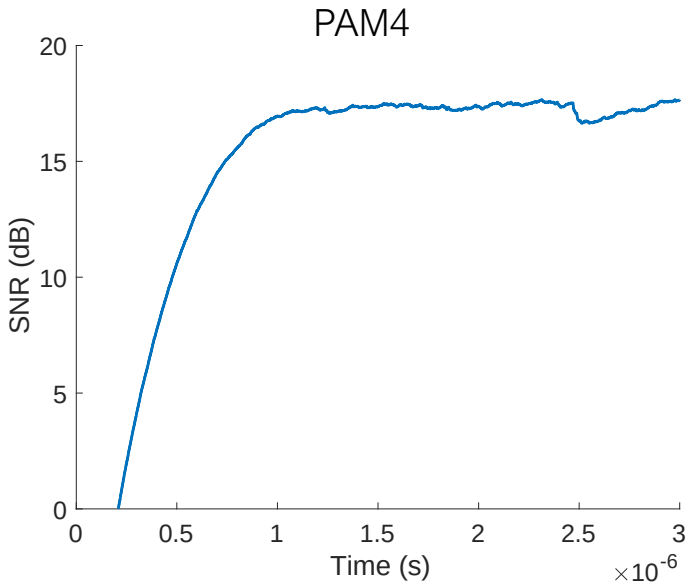


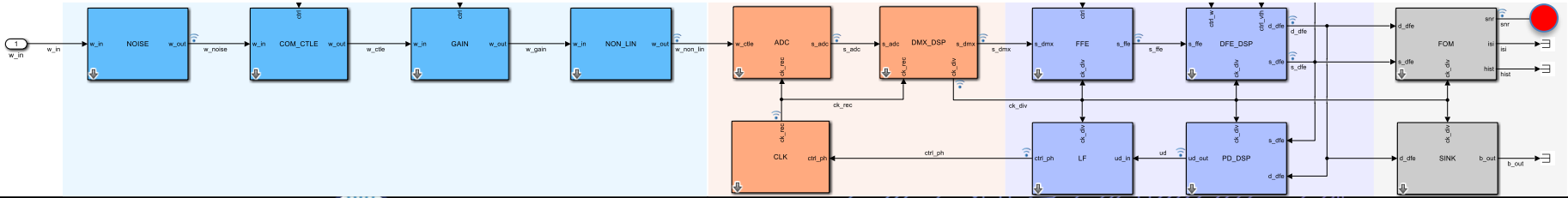




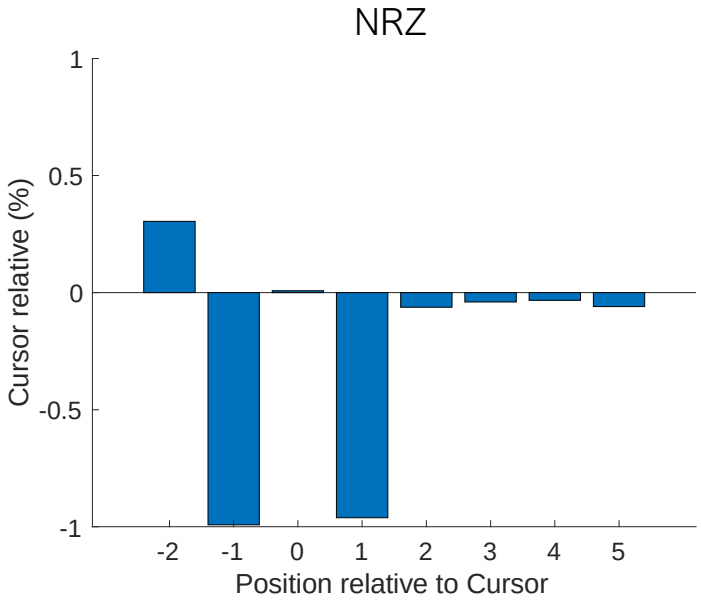
RX Model Observability: SNR

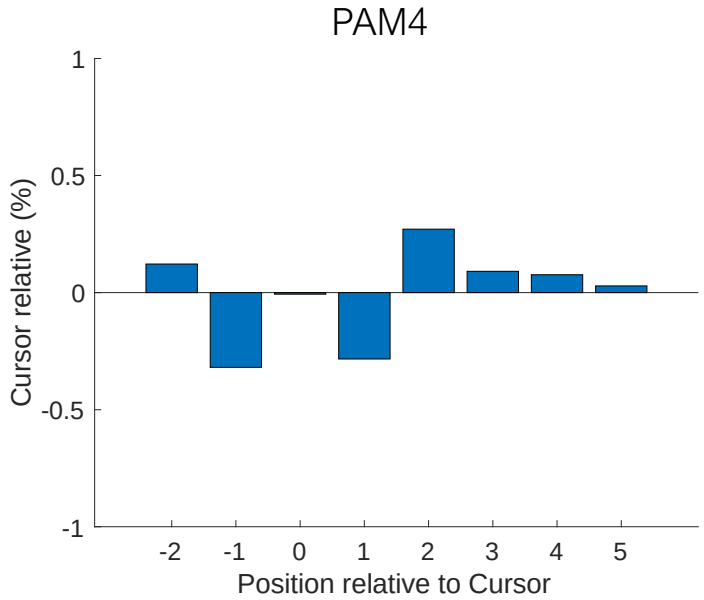


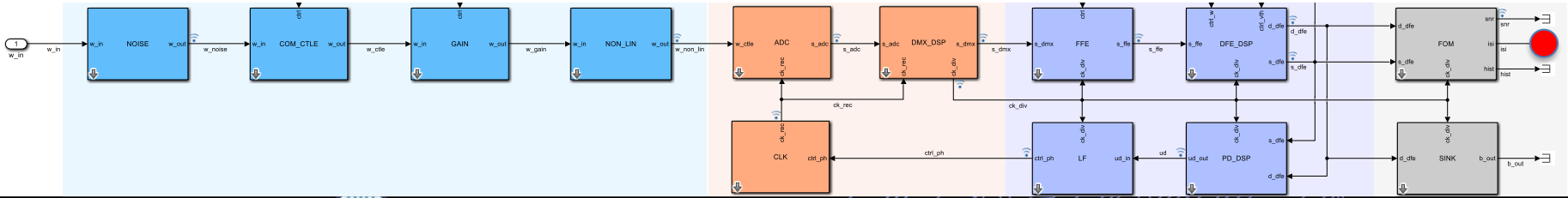




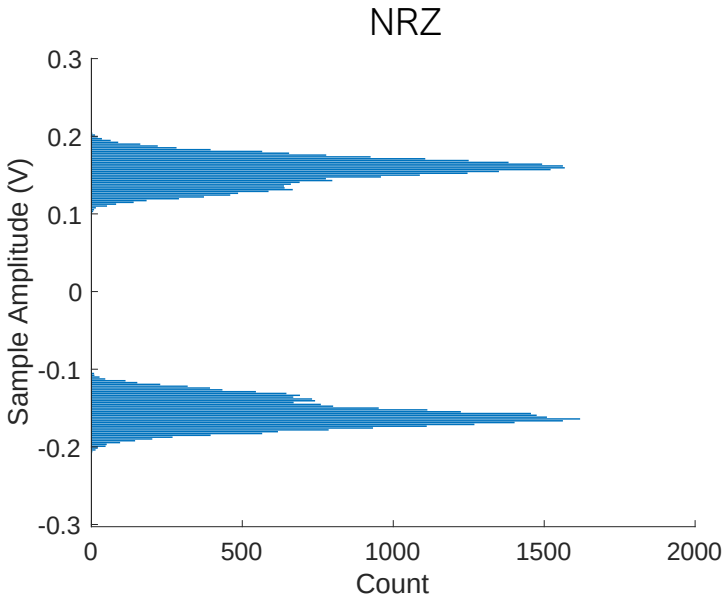
RX Model Observability: Residual ISI

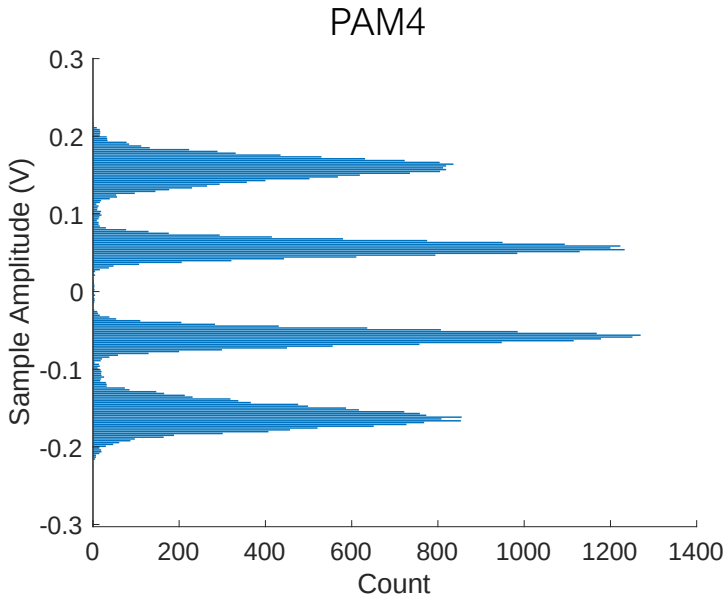


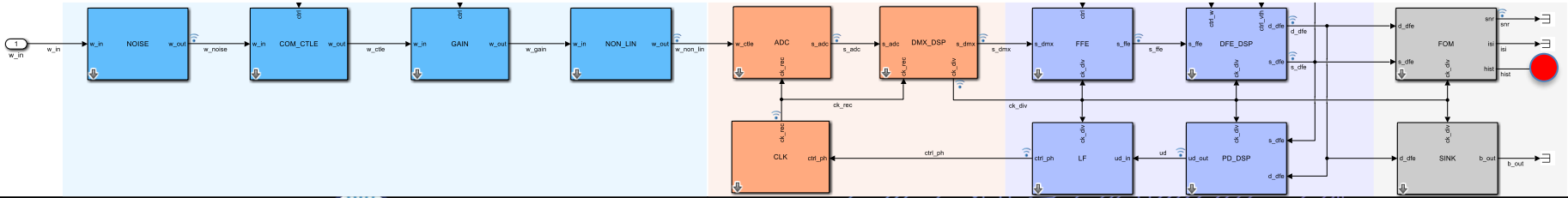




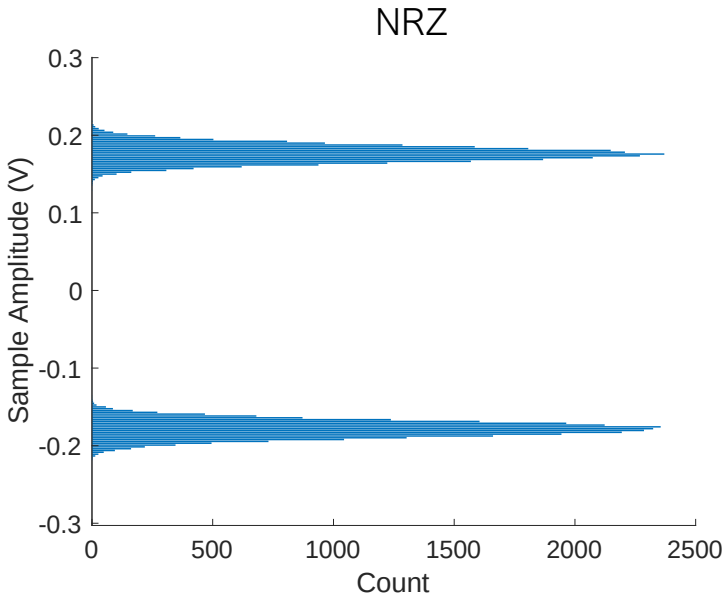
RX Model Observability: Amplitude Histogram

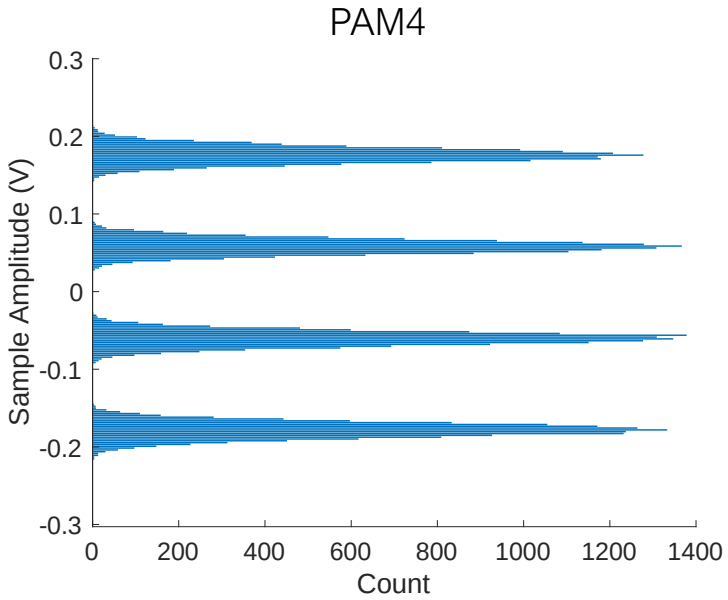


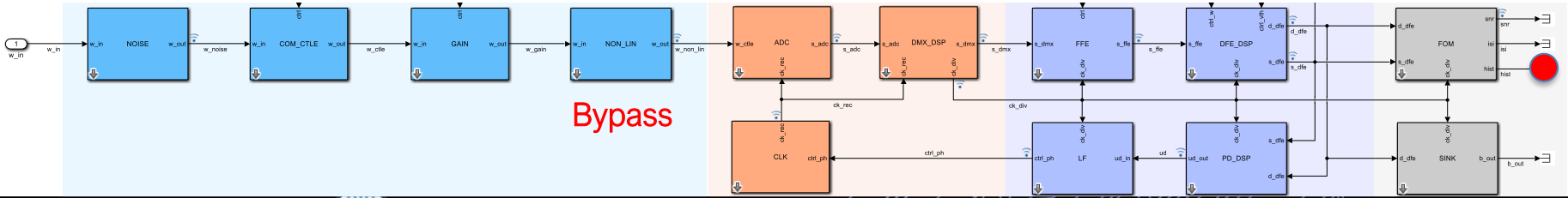




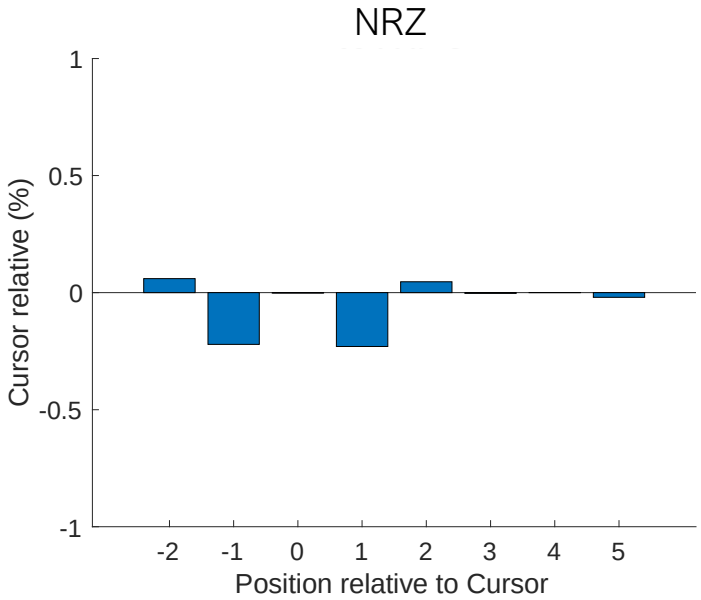
RX Model Observability: Non-Linearity OFF

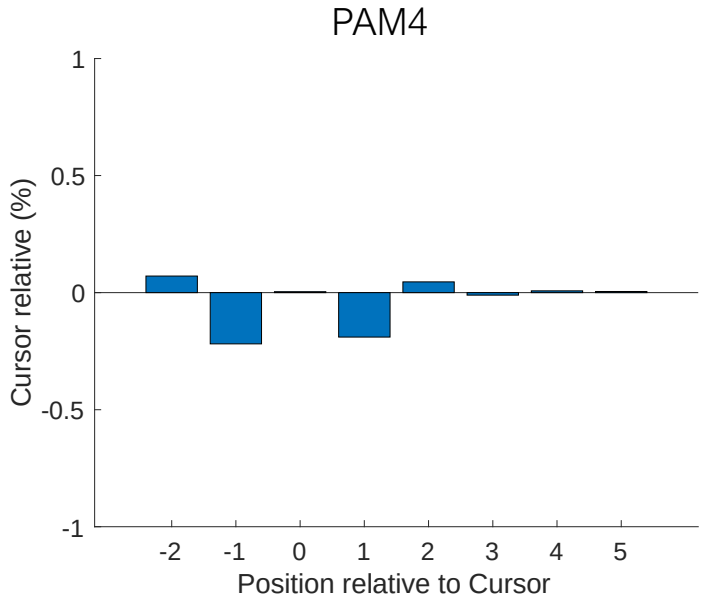


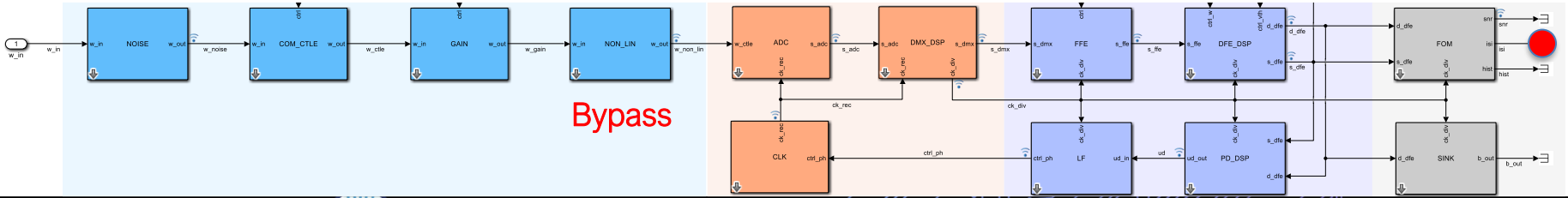




RX Model Observability: Non-Linearity OFF







RX Model Coverage and Configurability, 1 of 2

	COM	SeriaLink Model
Input-referred noise PSD	✓	✓
CTLE transfer characteristic	✓	✓
VGA gain range and step size	✗	✓
CTLE & VGA non-linearity	✗	✓
Number of clock phases	✗	✓
Clock jitter, residual phase mismatch	✗	✓
ADC time-interleaving depth, dynamic range	✗	✓
ADC nominal and effective resolution (ENOB)	✗	✓
Clock recovery loop dynamics	✗	✓

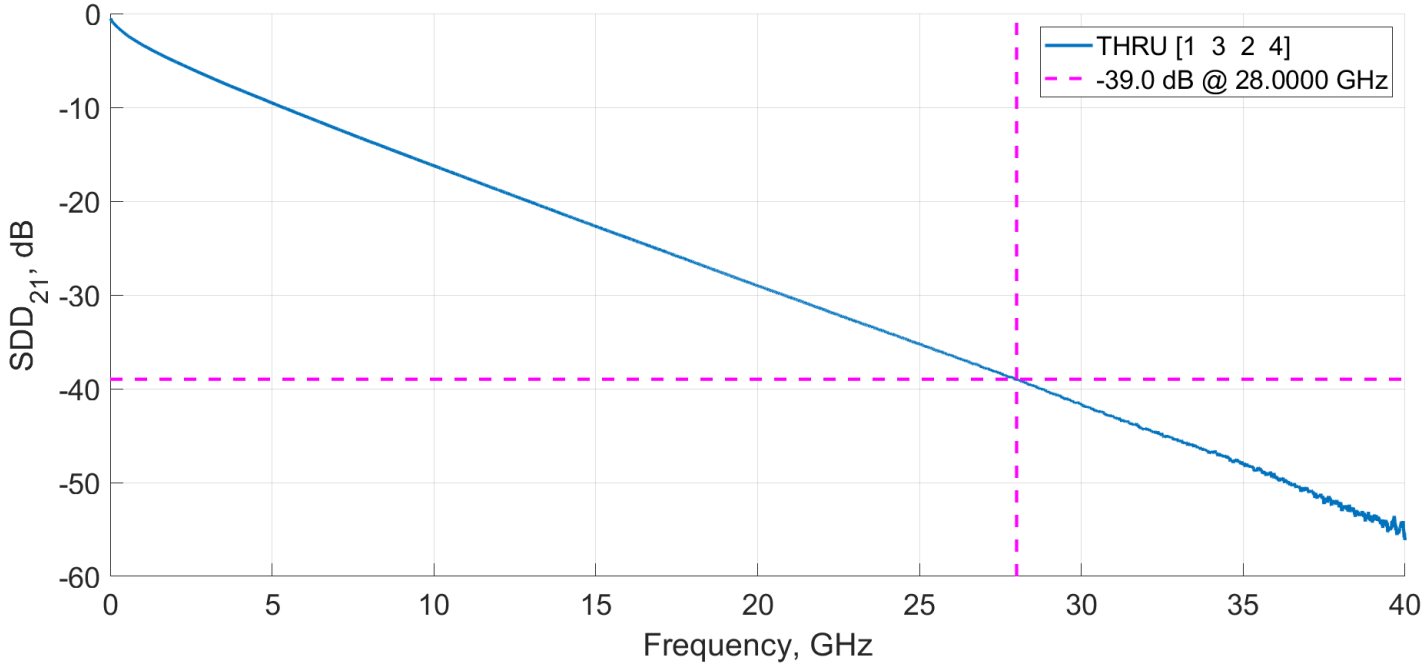
RX Model Coverage and Configurability, 2 of 2

	COM	SeriaLink Model
Number of FFE taps, tap ranges	✓	✓
Number of DFE taps, tap ranges	✓	✓
FFE and DFE resolution in DSP	✗	✓
DSP operating speed, sample demultiplexing depth	✗	✓
Latency due to sampling and demultiplexing	✗	✓
Phase detector pattern dependence	✗	✓
Interaction between phase recovery and adaptation loops	✗	✓
Representative time domain adaptation algorithms	✗	✓
Option to add FEC	✗	✓

Outline

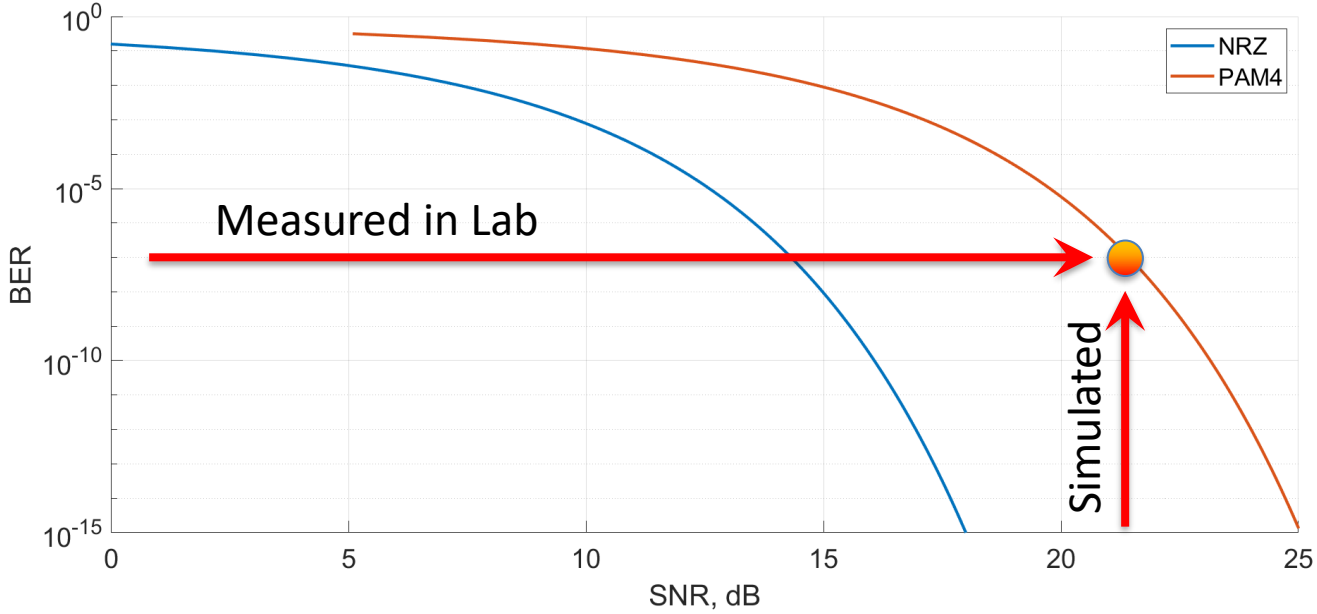
- Motivation
- System Modeling through SerDes Development
- Parametric DAC-based TX Model
- Parametric ADC-based RX Model
- **Model Correlation**
- Conclusion

Channel Response Used for Model Correlation



- Same channel was used in measurement and simulations for correlation purposes

Model Correlation Methodology at 112 Gb/s



- TX and RX configured consistently with SerDes IP and its corresponding IBIS-AMI model
- BER of 10^{-7} is measured in the lab, SNR of 21.5 dB is simulated using IBIS-AMI and SeriaLink models
- SNR-to-BER curve is used to establish correlation between SerDes IP and system models

Conclusion

- Explored system modeling in SerDes IP development
- Limited technical interaction between SerDes providers & system integrators due to lack of adequate models
- Proposed parametric SerDes system modeling framework – SeriaLink Model
- TX and RX modeling details enable looking inside COM implementation margin
- SeriaLink Model parametrization allows quick and simple model configuration to reflect actual SerDes IP
- Model observability is well beyond IBIS-AMI models, enabling channel / SerDes co-optimization
- SeriaLink Model allows code obfuscation at block level for IP protection, and for model sharing between teams
- Proposed model was correlated with 112 Gb/s SerDes using SNR and BER as correlation metrics

MORE INFORMATION

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